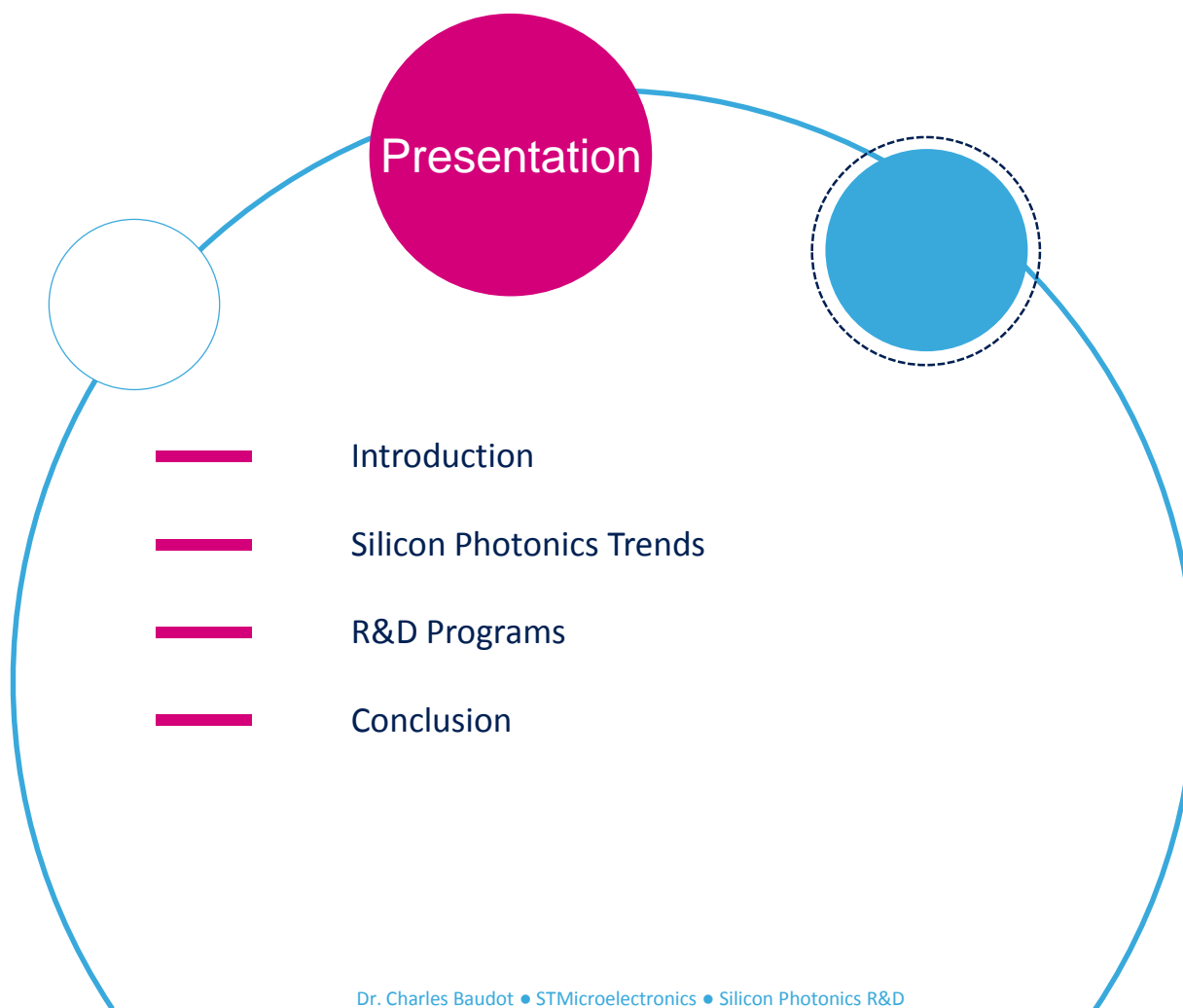




Addressing future trends in integrated silicon photonics

Charles Baudot

Silicon Technology Development – Process Integration
STMicroelectronics (Crolles 2) SAS - France



Silicon Photonics: Rationale

3

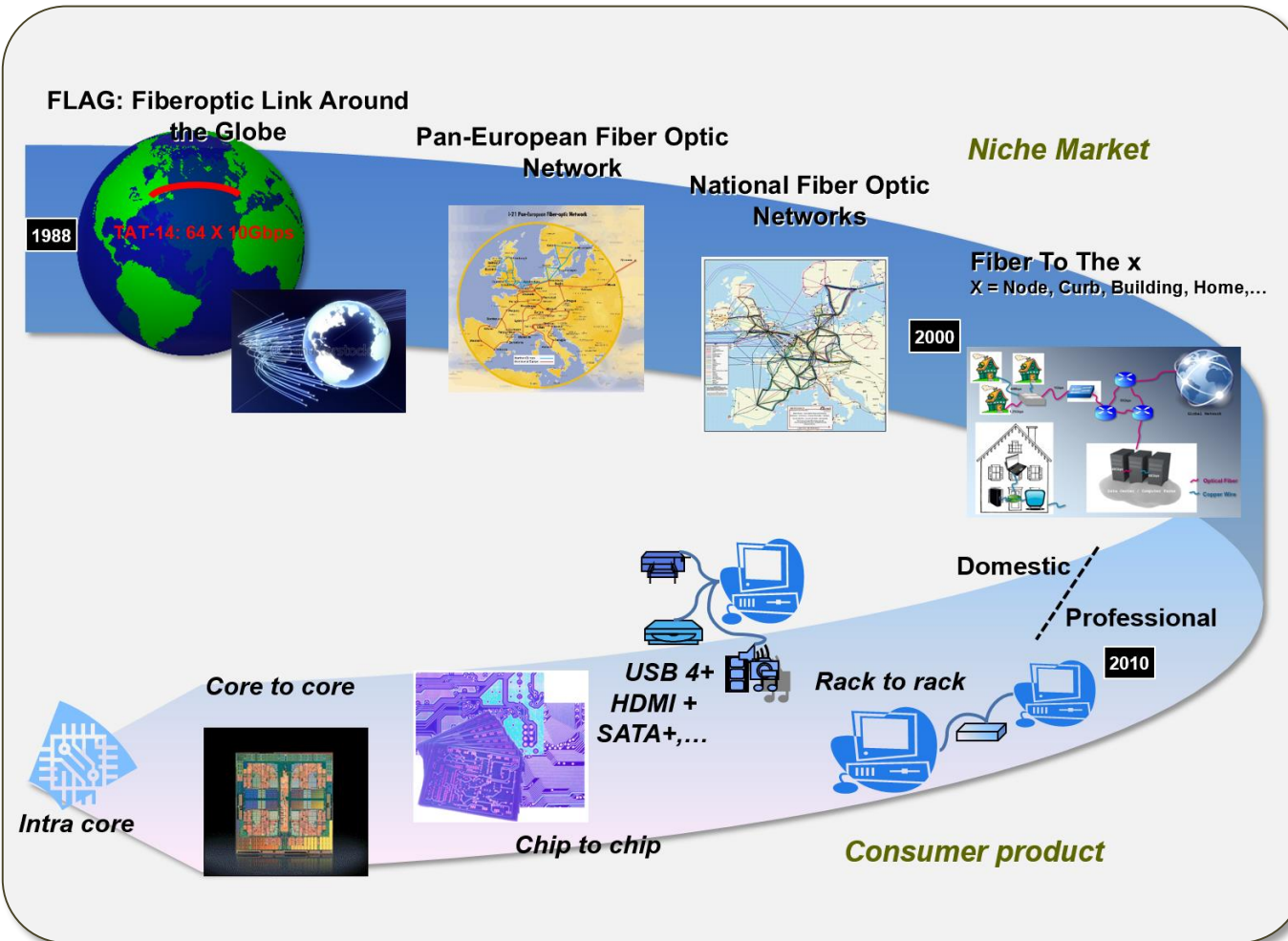
What's the big idea about silicon photonics?

- **What:**
 - Integrated photonic circuits on silicon using CMOS foundry facilities
- **Why:**
 - Cost of production
 - Power consumption efficiency
 - System footprint
 - Alternative market not fully addressed by III-V discrete photonics
 - New markets out of data-communication
- **Opportunities:**
 - Knowhow → Among the more explored & mastered areas of science
 - Throughput → Large volume manufacturability
 - Robustness → Resist to a wide variety of perturbations
 - Reliability → Long lifecycle when operated within specifications
- **Constraints:**
 - Process flow → Fabrication flow must be compatible with existing technologies
 - Contamination → Strict regulations about: material contamination, health hazards, safety hazards
 - Some materials not allowed (III-V, Fe,...)
 - Some materials in restricted zones (FEOL / BEOL : Cu, Au,...)

Optical Communication Trend

4

Fiber optics data communication evolution



Optical link network keeps on getting denser.

So far, the market still addresses the professional market.

Projections tend towards intra processor core optical communication.

Ultimately, we may converge towards a model where:

Logic → Electrical charges

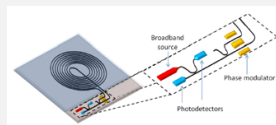
Communication → Photons

Storage → ions

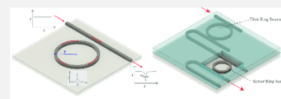
Datacom & More Than Datacom

5

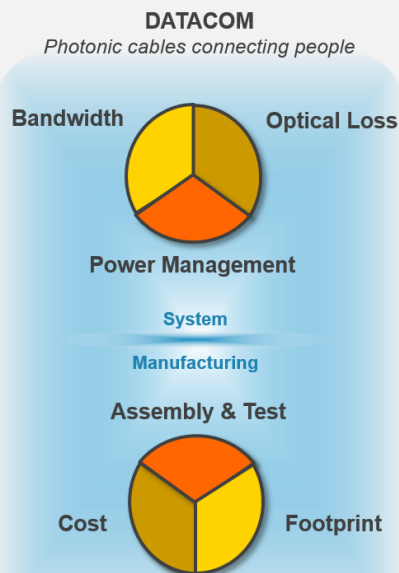
New opportunities in silicon photonics



Hybrid silicon waveguide optical gyroscope
John Bowers et al.



Silicon-Based Optical Biosensors
Laura Lechuga et al.

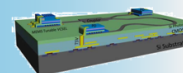


More than DATAKOM

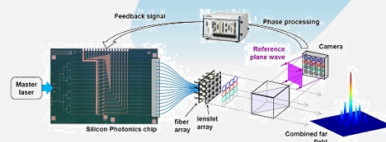
Photonic sensors & detectors connecting objects



LAser Detection And Ranging
Ming Wu et al.



Atmospheric LiDAR anemometer
Jérôme Bourderionnet et al.



Silicon photonics cannot rely on data communication professional market only.

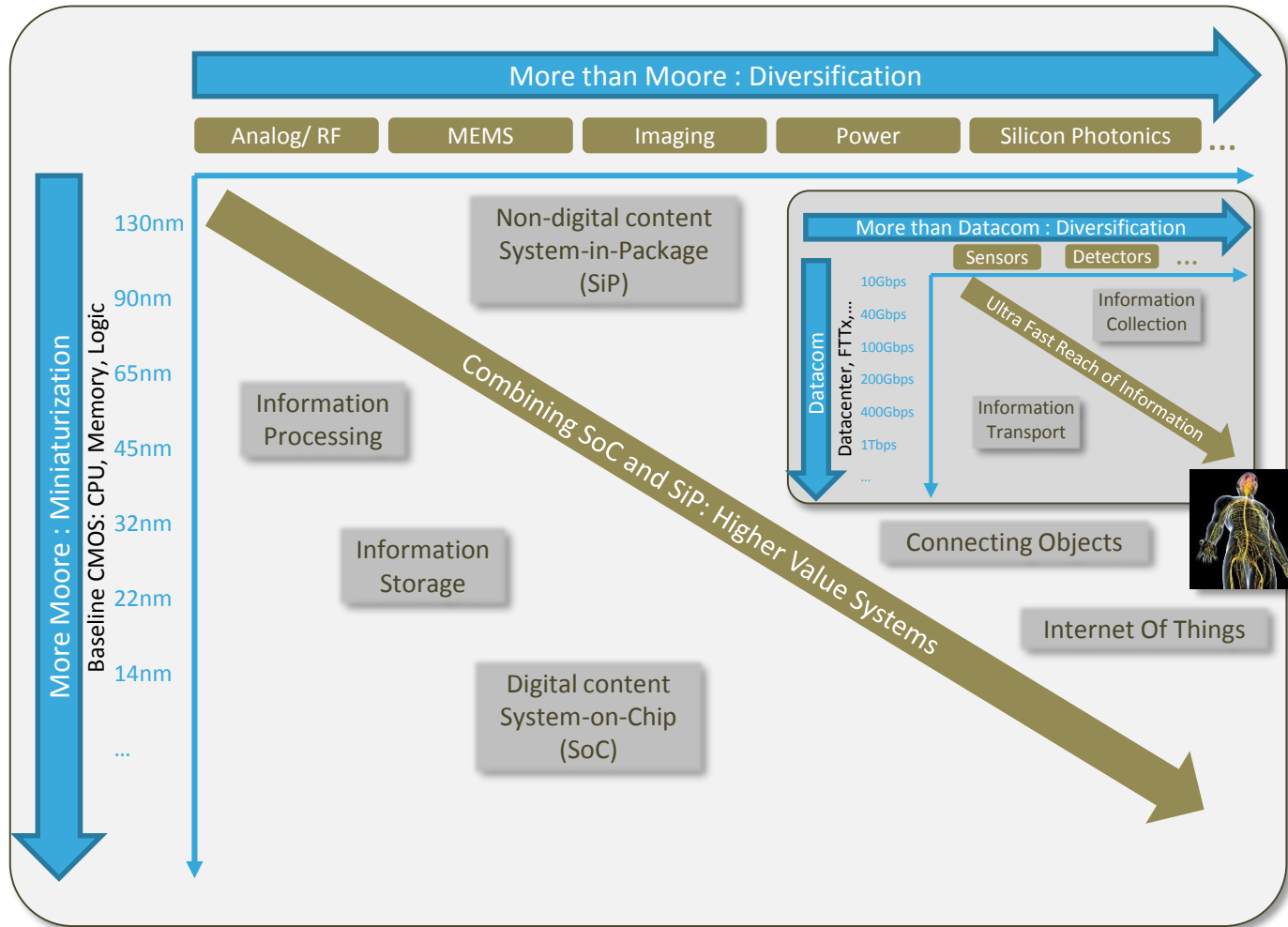
For the industry to develop:

- More applications
- Huge volumes
- More actors
- Bigger competition
- Lower prices
- More innovation

Silicon Roadmap

6

Silicon Photonics: A roadmap in the roadmap



Mixing up future silicon photonics systems will potentially lead to even better innovation:

Typically, a trend in automation is to have robots substituting to humans. Digital logic + photonics communication + photonics sensor \equiv neuronal network + nervous network.

- ➔ Rapid detection, rapid dispatch, rapid analysis of information.
- ➔ Applications: Autonomous cars, airplanes, trains,...



R&D Programs:

plat**4M**

FP7 Project 2013 - 2017

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TNO
MENTOR GRAPHICS
PHOENIX
III-V LABS
UNIVERSITY COLLEGE CORK, Tyndall
POLYTEC
THALES
UNIVERSITE PARIS-SUD
AIFOTEC FIBEROPTICS
NXP SEMICONDUCTORS
SI2

PLAT4M - FP7 Project

- **Project full title:** " Photonic Libraries And Technology for Manufacturing "
- **Project Description:** PLAT4M's objective is to bring existing silicon photonics research platform to a maturity level which enables seamless transition to industry, suitable for different applications fields and manufacturing volume levels.

CEA-LETI

SYLPHIDE
200mm
MPW

IMEC

ISIPP25G
200mm
MPW

STMicroelectronics

DAPHNE
300mm
R&D Platform

Tyndall National Institute

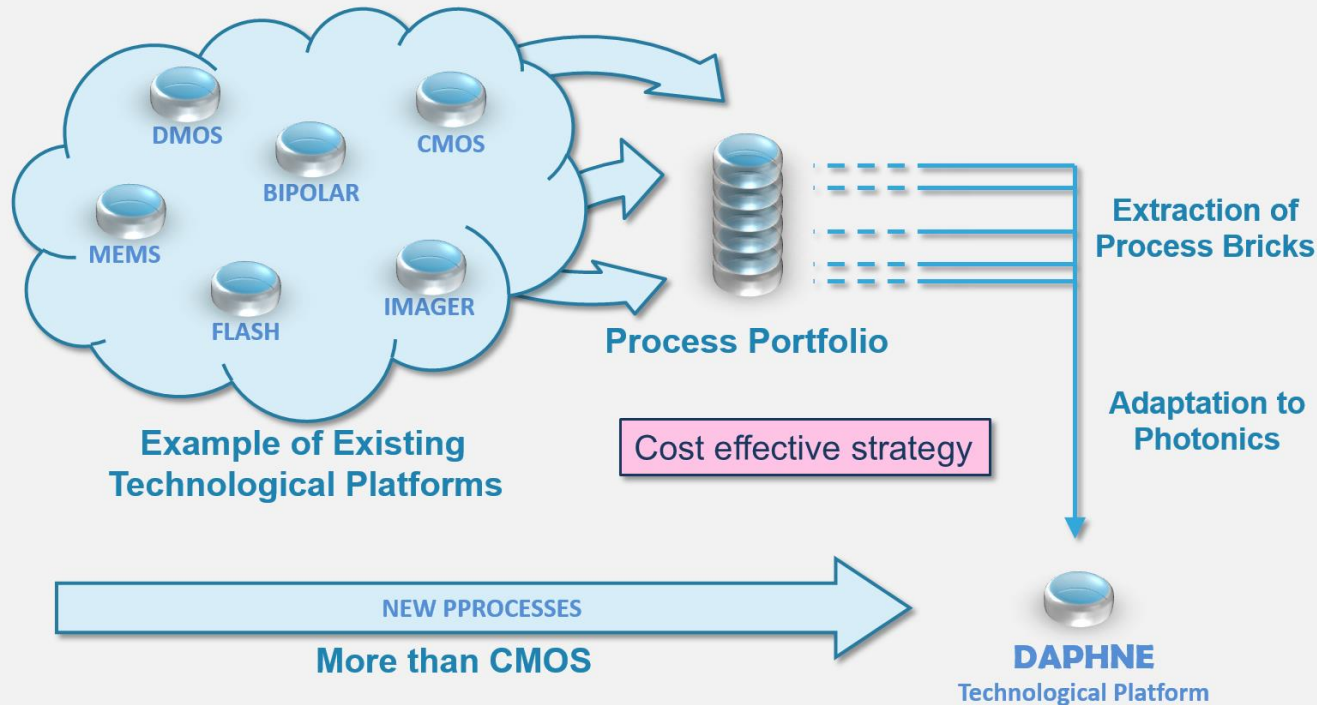
Assembly &
Packaging
Solution



Technology Setup

9

Building up a new technology



Derivative technologies (diversification) are usually launched using existing processes

DAPHNE (Datacom Adv. Photonics Nanoscale Env.) is a technology meant for R&D.

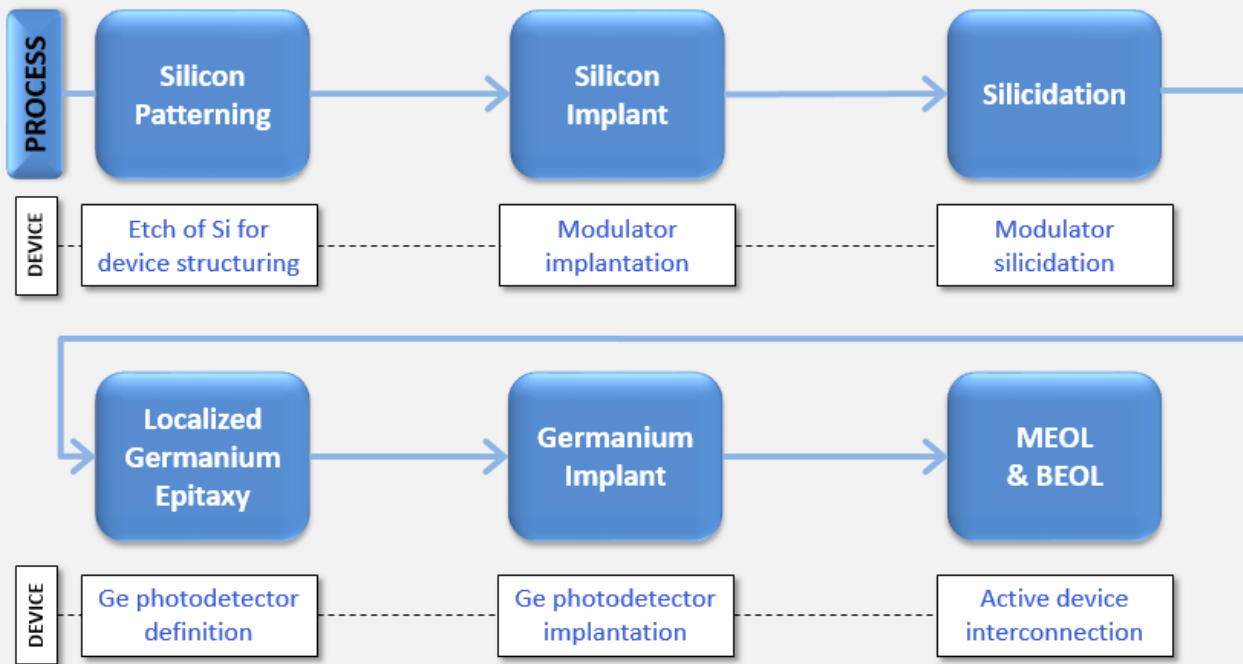
Both the process and device library evolves.

The current and predicted production volumes are the main arguments that usually decide about the amount to be invested in innovation.

Fabrication Flow

10

Process building blocks compatible with a CMOS foundry



Process:

The fabrication flow is divided in building blocks so that process development work is done in parallel. The integration activity ensures that the blocks are compatible with each other.

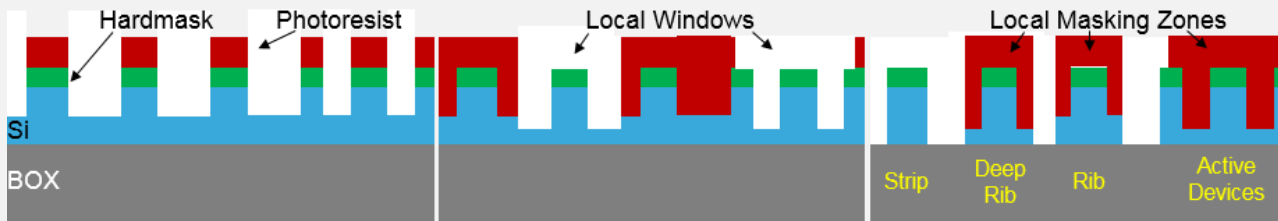
Device:

While passive devices are all fabricated in a single block, active devices involve the whole flow.

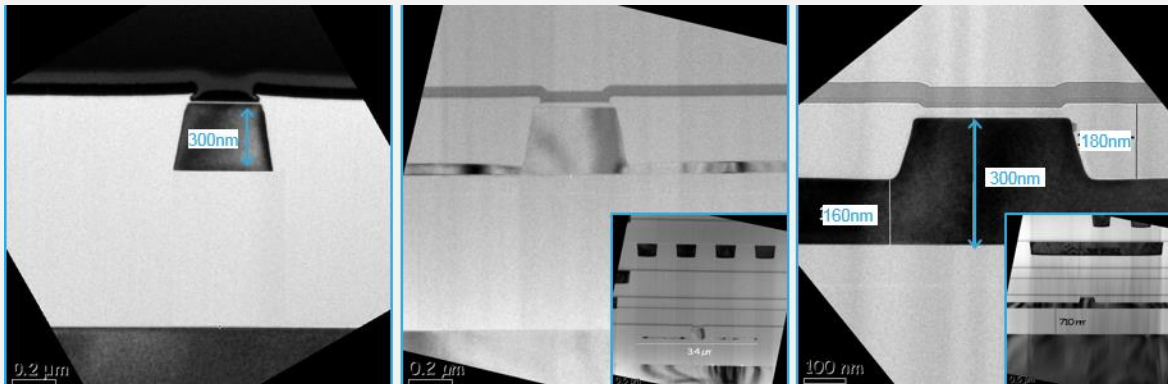
Silicon Patterning

11

Photonics Integrated circuits



- Step 1:
 - High resolution patterning step to define the global photonic path in a single step (auto-alignment)
- Step 2:
 - Low resolution patterning step to locally etch further silicon
- Step 3:
 - Low resolution patterning step to locally protect silicon from etching



350nm strip
IL: 3.5 dB/cm

320nm deep-rib + 50nm slab
IL: 3.7 dB/cm

400nm mid-rib + 160nm slab
IL: 1.4 dB/cm

The inset shows the waveguide after the whole process

Target:

Etch silicon so as to define photonic devices & circuits

Challenge:

Auto-alignment between all devices at chip level

Partial etching of silicon with good uniformity

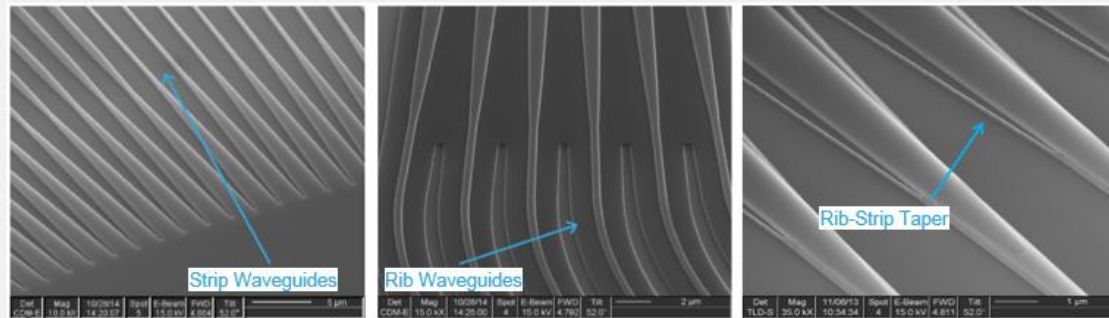
Non-Manhattan architectures

Huge disparity in targeted lateral dimensions & morphologies

Silicon Patterning

12

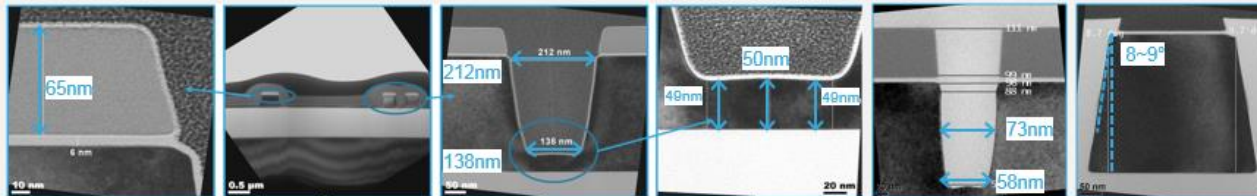
Multi-level silicon patterning development to address device requisites



Strip waveguides with 150nm minimum spacing

Rib waveguides with 310nm minimum spacing

Rib-to-strip tapers with an auto-alignment tip of 250nm on top of the rib



TEM observation of the remaining hardmask on top of rib regions

Deep-rib waveguides observed in a ring device

Observation of the trench between the ring and the linear waveguide

Measured thickness in the deep-rib dense slab region

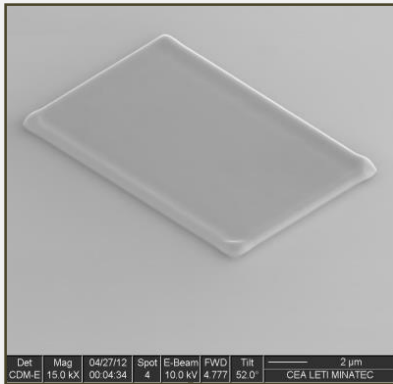
Measurement of a dense trench targeted during the first patterning step

Etch profile measured on an isolated strip waveguide

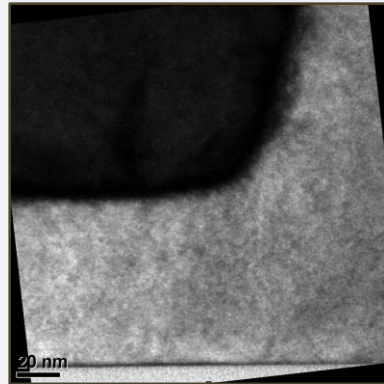
Germanium Integration

13

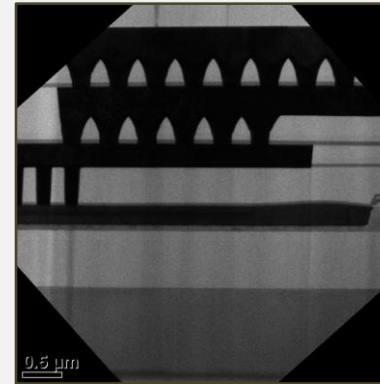
High Speed Photodetector



(10 X 15) µm pure mono-crystal Ge obtained by selective epitaxial growth using a patterned silicon seed masked by silicon dioxide



Interface between germanium and silicon layers showing a good Ge crystal quality



Right part of Ge pin photodiode with 3 interconnect metal layers

New material integration is a challenge in a CMOS foundry. Besides contamination issues, process feasibility must be established.

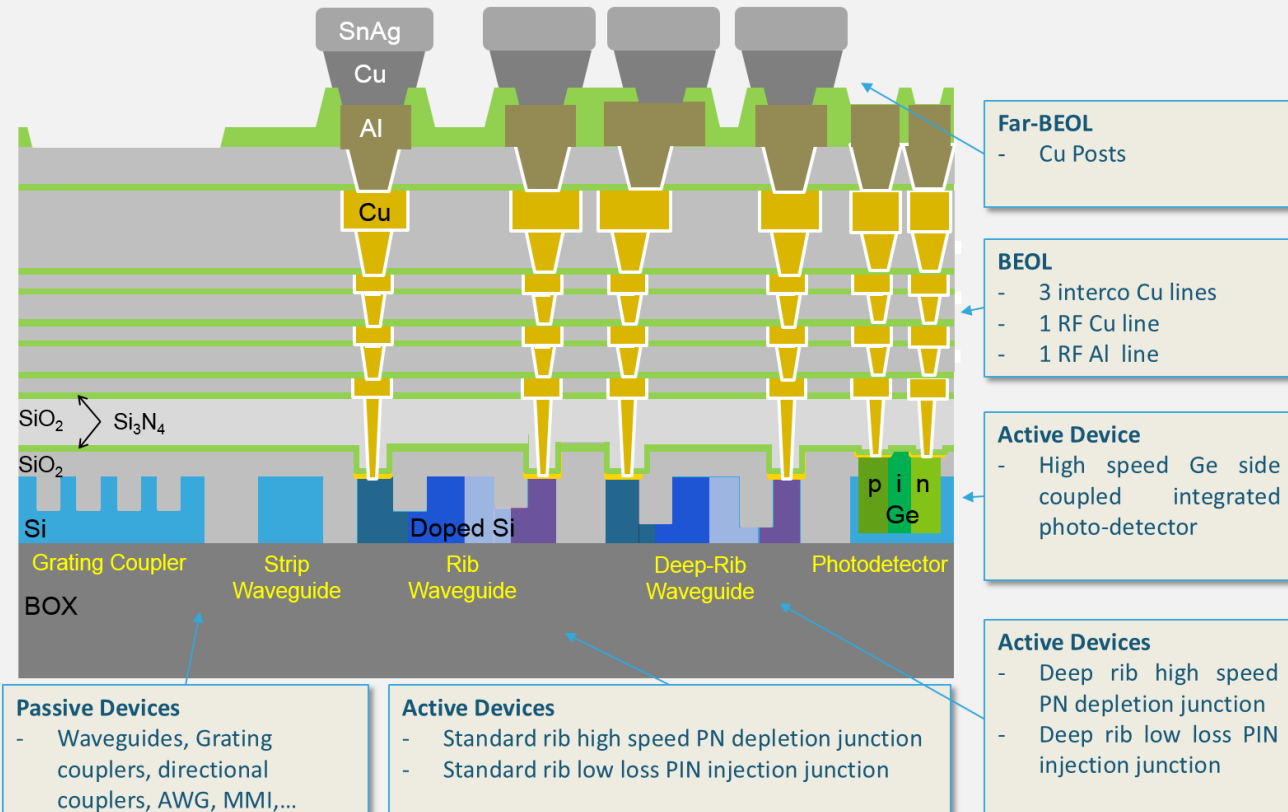
Mono-crystalline germanium includes:

- Selective epitaxial growth of Ge using a Si seed masked by SiO₂.
- Si/Ge lattice mismatch.
- Thermal budget of Ge
- Chemical compatibility (Ge oxidizes easily. GeO_x is soluble in water)
- Same implantation strategy as silicon.
- Same BEOL of Si devices.

Photonic Integrated Circuit

14

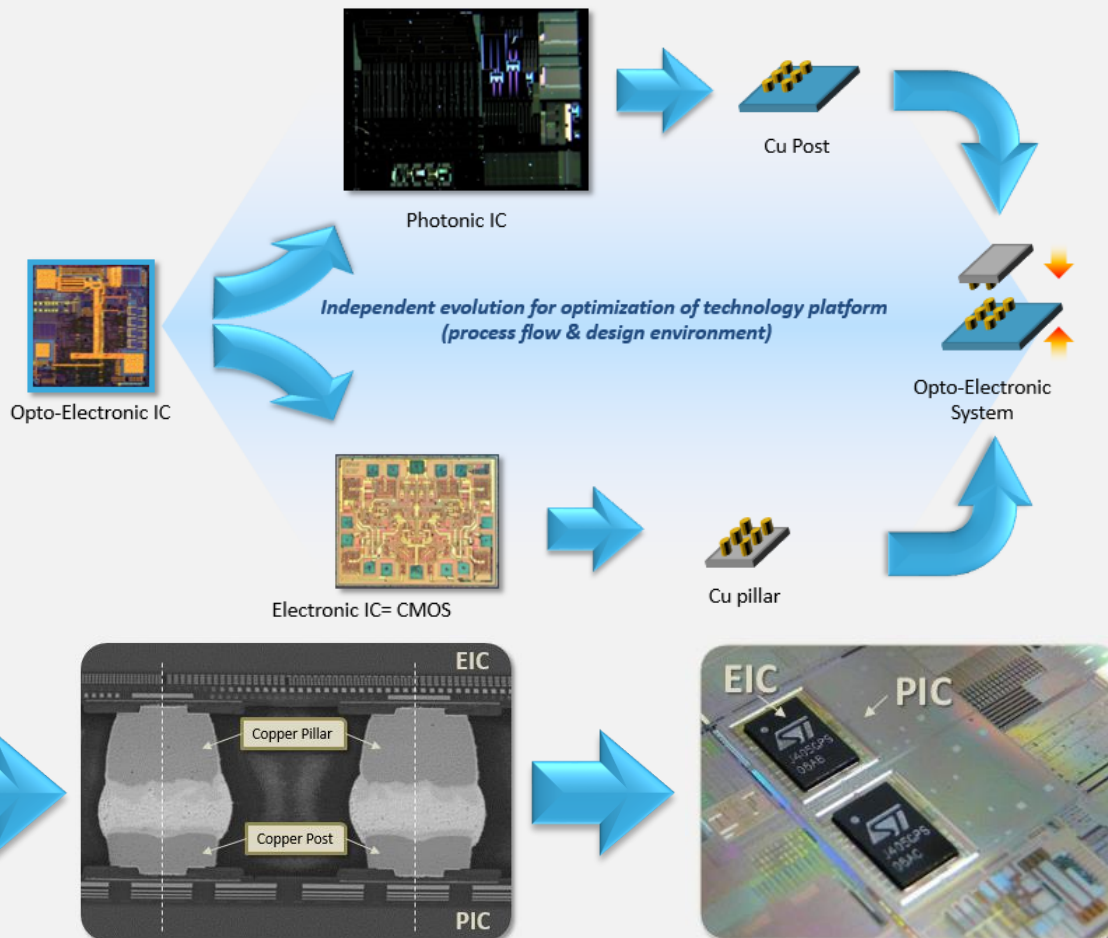
Schematics of a typical PIC



System Integration

15

3D integration of EIC & PIC



Copper posts and copper pillars are grown on the metal pads.

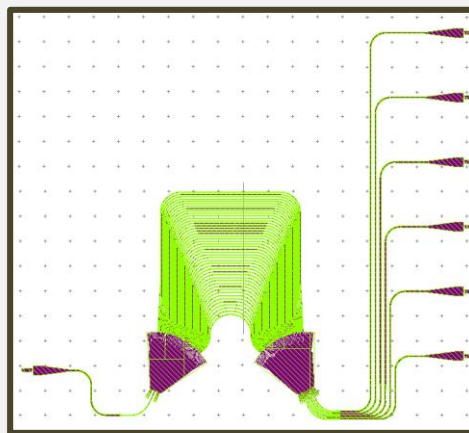
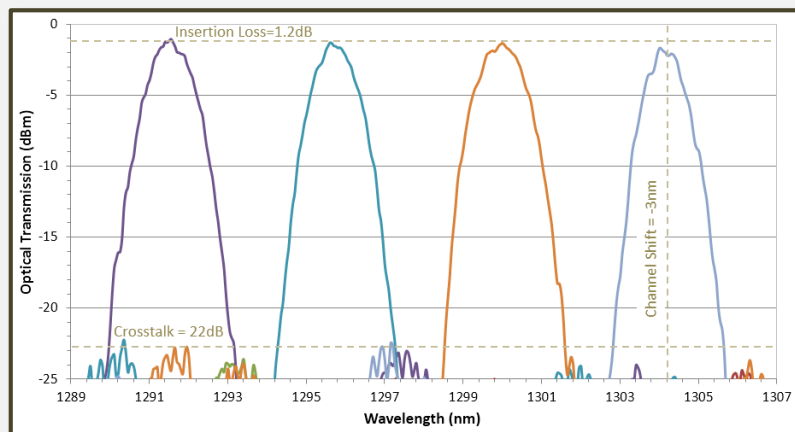
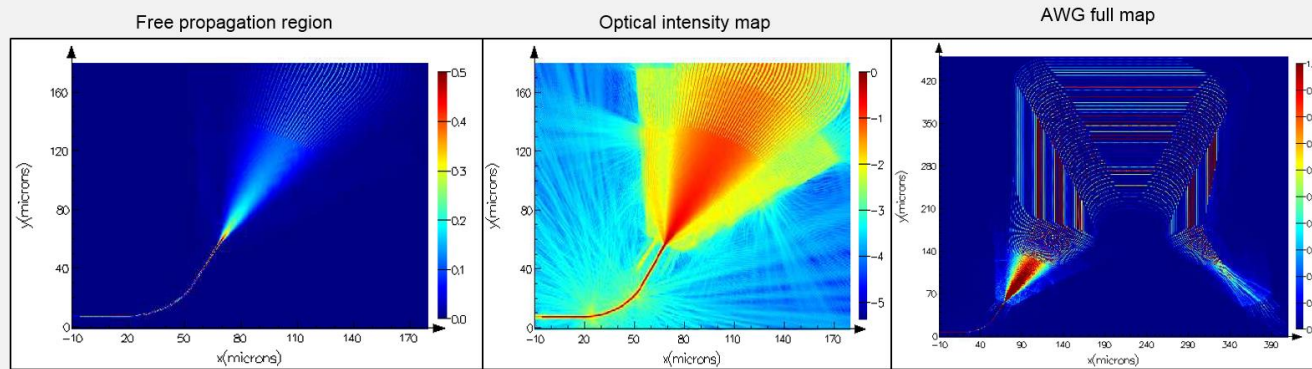
Bonding is done by die-to-wafer flip chip of the EIC on the PIC.

Copper pillars allow direct connection between the middle of the two dies (No routing to die edge).

Test Vehicle: 100GBase-LR4 Demo

16

Integrated Multiplexed Transmitter



100GBase-LR4 transceiver system.

WDM device designed and simulated: Array Waveguide Grating.

Stand-alone device shows a loss of 1.2 dB / channel

Device integrated in system. Fabrication On-going.



IRT Project 2012 - 2018

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STMICROELECTRONICS STD CROLLES

MENTOR GRAPHICS

SAMTEC

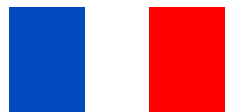
CNRS

R&D Programs:



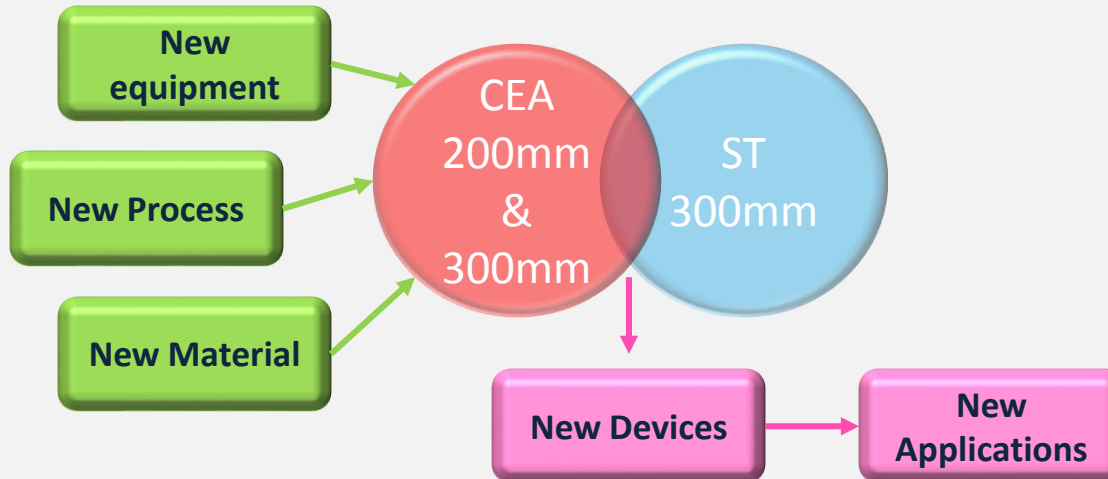
Institut de recherche
Technologique Nanoelec

Funding:



IRT – Nanoelec Project

- **Project full title:** " Institut pour la Recherche Technologique "
- **Project Description:** Bring together in a single organization all the tools and know-how to develop silicon photonics solutions that can address a wide variety of applications.

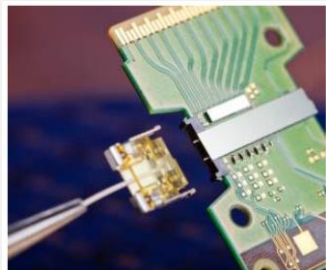


Silicon Photonics & III-V Integration

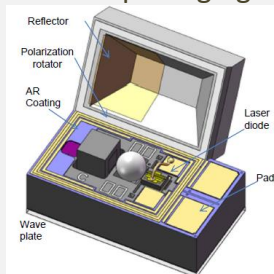
19

Does it make sense?

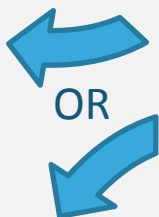
Integration of III-V laser coupled to silicon waveguide at wafer level



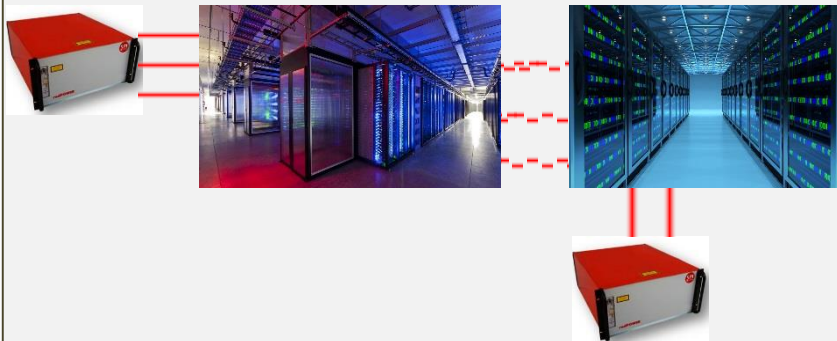
3D Integration of LaMP module at packaging Level



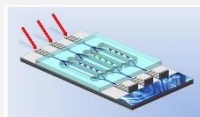
DATAKOM



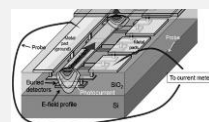
Central optical carriers distributed at higher system level



DIVERSIFICATION



Lab On Chip
System On Chip
Bio-Chemical Detection
...



It is not clear yet whether an integrated laser at wafer level will correspond to all needs in optical data communication.

System providers militate in favors of different approaches.

Main parameters for DATAKOM:

- Cost
- Footprint
- Power consumption
- Reliability
- Robustness

In alternative markets, the constraints are different. Moreover, the need of an integrated source is very likely.

Source Integration

20

Integrated III-V Laser

Typically $3\mu\text{m}$ thick III-V bonded to SOI waveguide.

Close proximity ($\sim 100\text{nm}$) needed between III-V and Si 500nm waveguide.

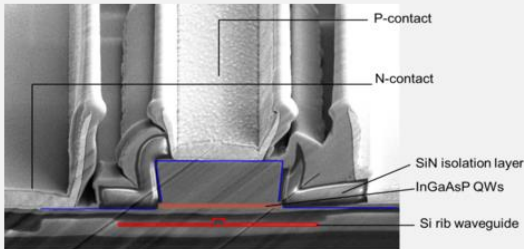
Surface preparation prior to bonding based on CMP, preventing topography on Si photonics wafer.

Topographical problem: similar heights ($\sim 3\mu\text{m}$) of laser and 4 level metal stack.

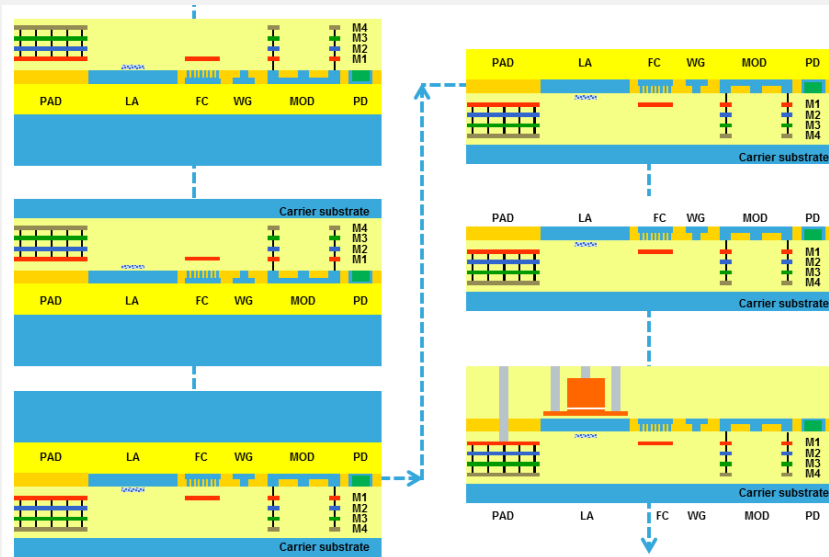
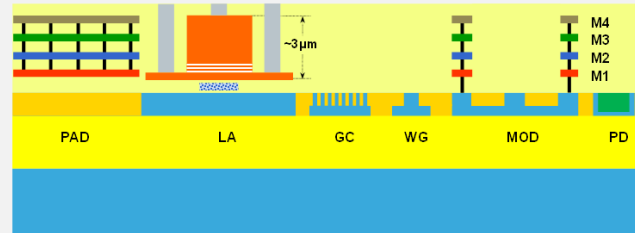
Planar surfaces needed (CMP) for III-V/Si bonding and 4 level Cu back-end.

The idea : use flat back-side of Si waveguide for laser integration.

Si device interconnects on one side, III-V/Si laser on other side.



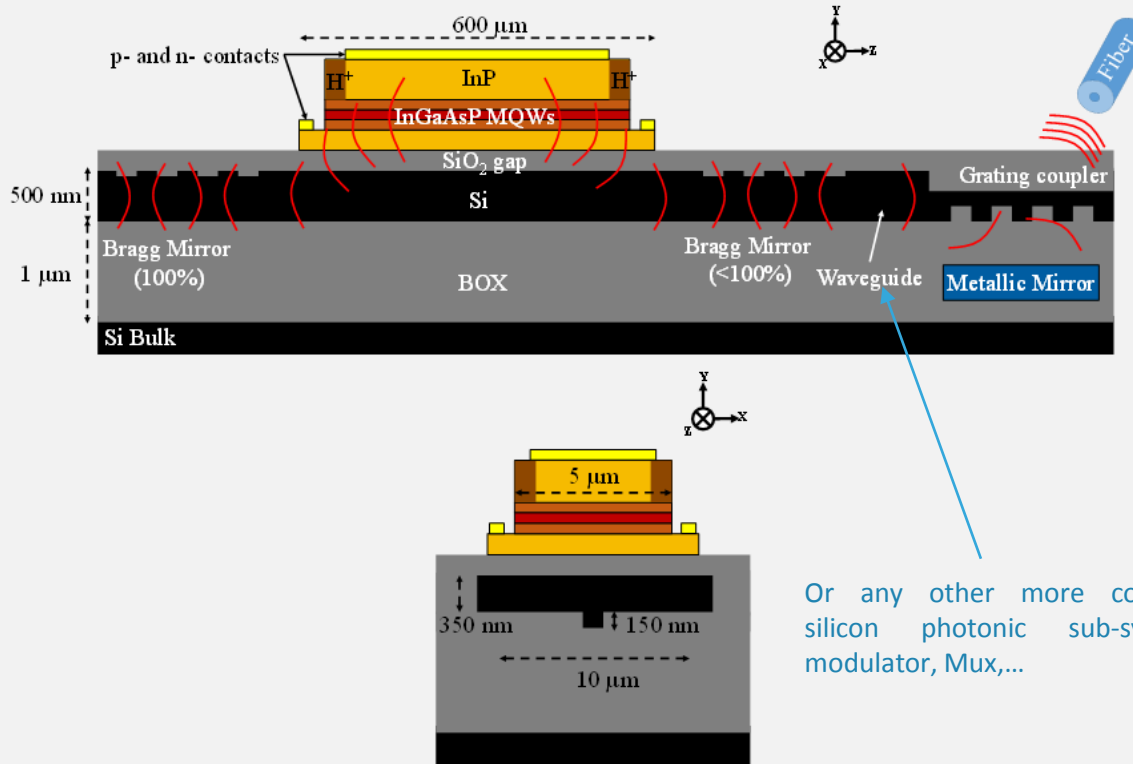
CEA-LETI integration: State-of-the-art III-V laser integration in silicon photonics



Source Integration

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Integrated III-V Laser



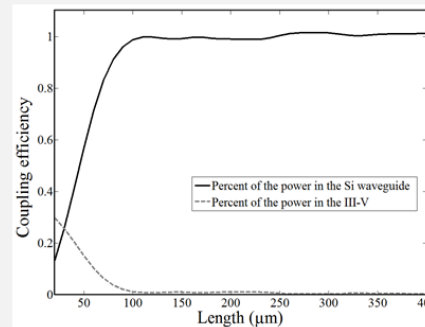
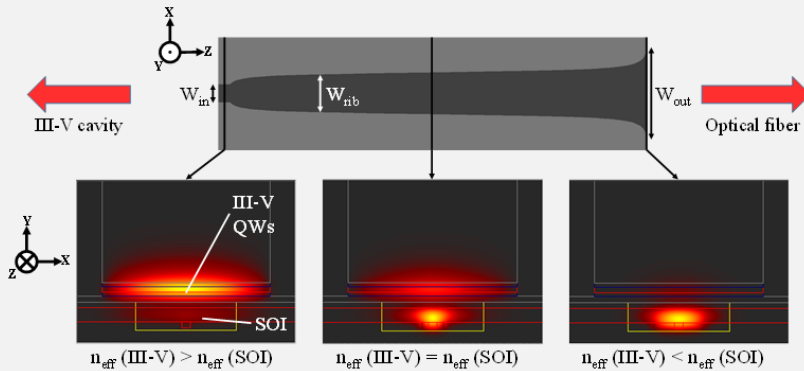
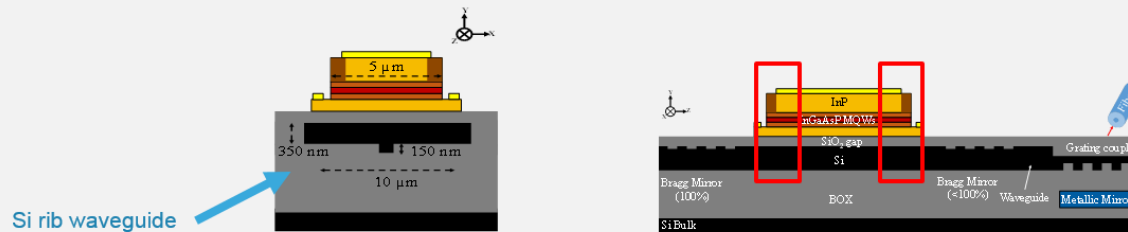
Distributed Bragg Reflector hybrid III-V/Si laser cavity emitting at 1310nm

Active region : optical mode confined in the III-V waveguide

Mirror: DBRs in the Si on both side of the III-V

Or any other more complex silicon photonic sub-system: modulator, Mux,...

Integrated III-V Laser



Light transferred by adaptation of effective index using the super-mode theory*:

Variation of the SOI waveguide rib's width (W_{rib}) along the propagation direction.

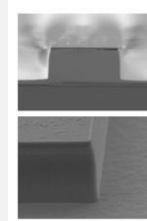
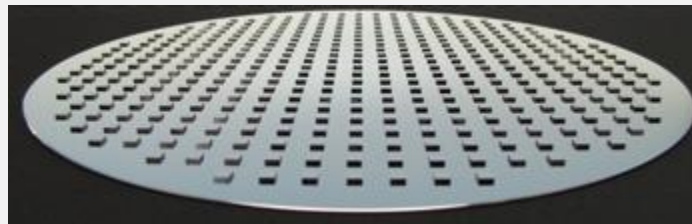
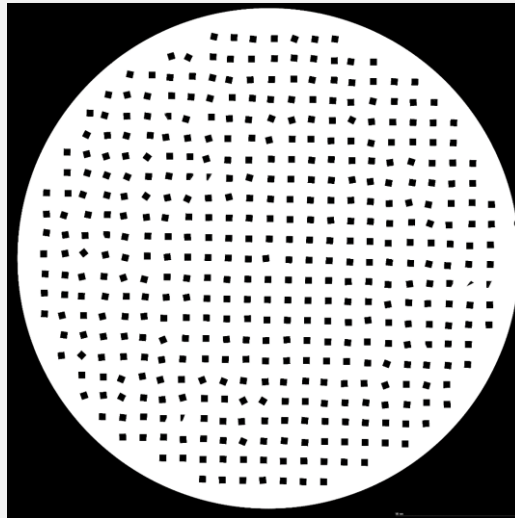
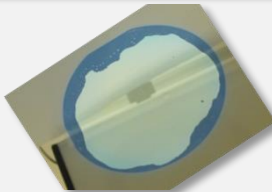
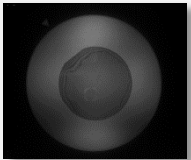
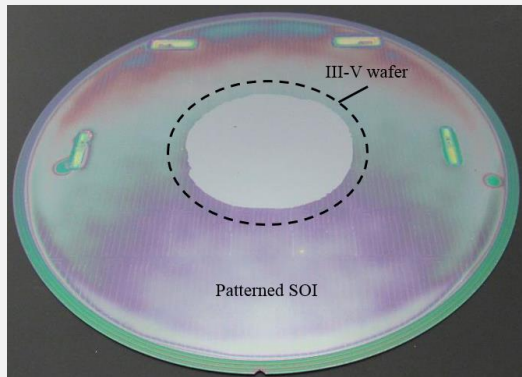
Over 97% of the light is transferred to the single-mode waveguide

* X. Sun, H.-C. Liu, and A. Yariv, "Adiabaticity criterion and the shortest adiabatic mode transformer in a coupled waveguide system," Opt. Lett. 34, 280-282 (2009)

Source Integration

23

Integrated III-V Laser



SOI wafer level III-V bonding strategy:

Preliminary tests done by wafer-to-wafer bonding

Ongoing developments to bond locally patches of III-V material

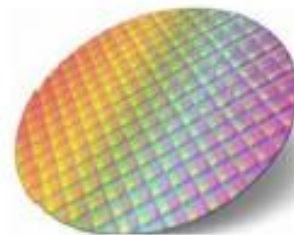


H2020 Project 2015 - 2018

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STMICROELECTRONICS MPD AGRATE
UNIVERSITY OF PAVIA
VARIO-OPTICS
SEAGATE SYSTEMS (UK) LTD.
UNIVERSITY OF SOUTHAMPTON, ORC
UNIVERSITY OF ST ANDREWS
FINISAR

R&D Programs:



COSMIC€

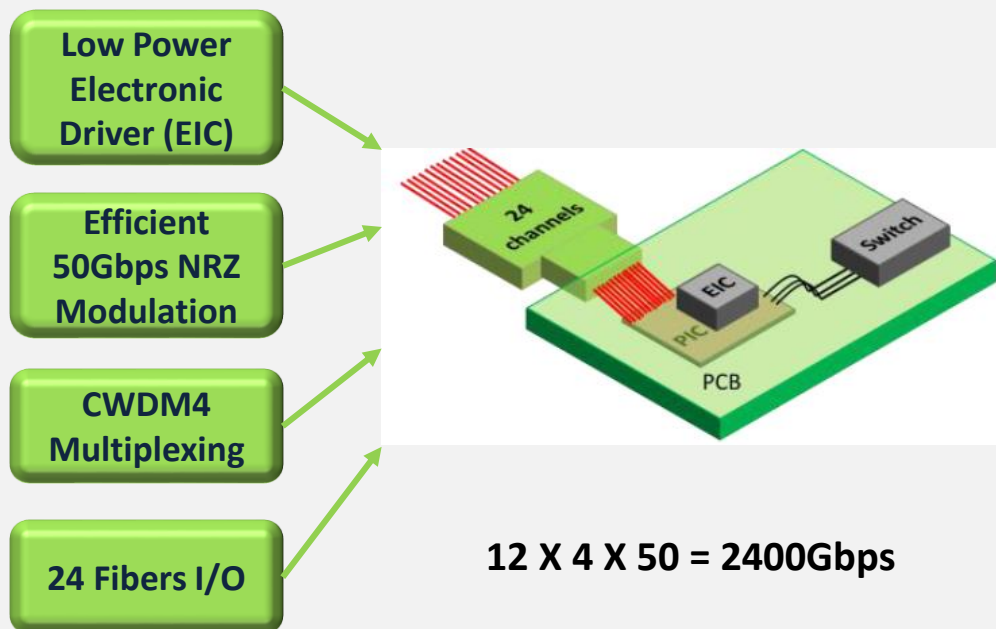
CmOs Solutions for Mid-board Integrated transceivers with breakthrough Connectivity & ultra low Cost (COSMICC).

Funding:



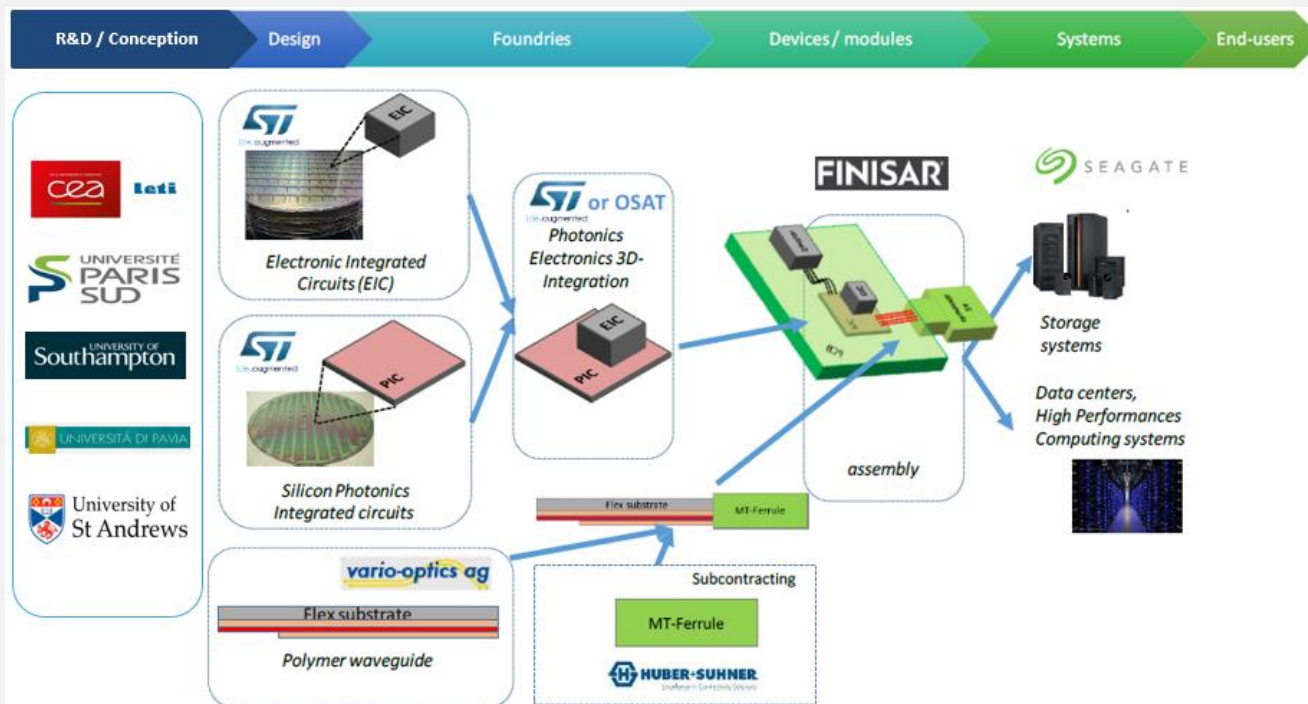
COSMICC-H2020 Project

- **Project full title:** " CmOs Solutions for Mid-board Integrated transceivers with breakthrough Connectivity at ultra-low Cost "
- **Project Description:** COSMICC consortium will achieve mid-board optical transceivers in the [2Tbit/s, 2pJ/bit, 0.2\$/Gbit/s cost]-range.



COSMICC-H2020 Project

Project Organization:

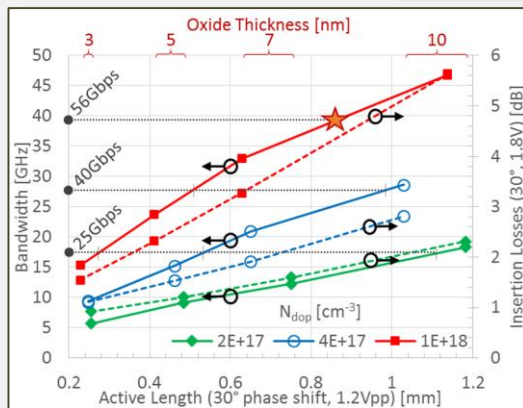
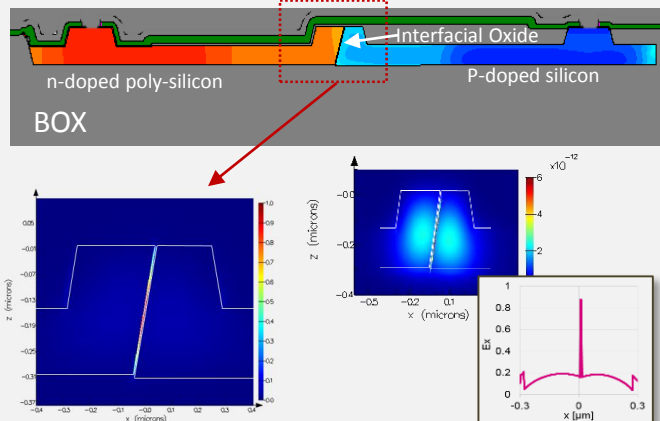


Capacitive Modulators

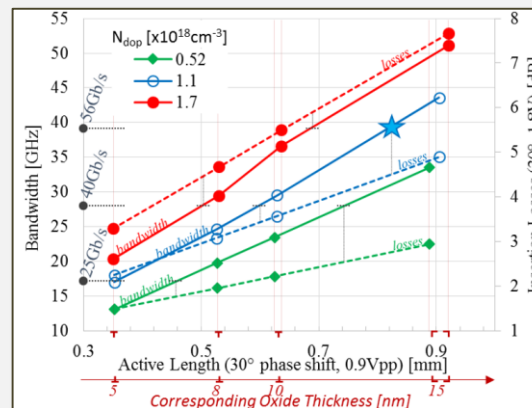
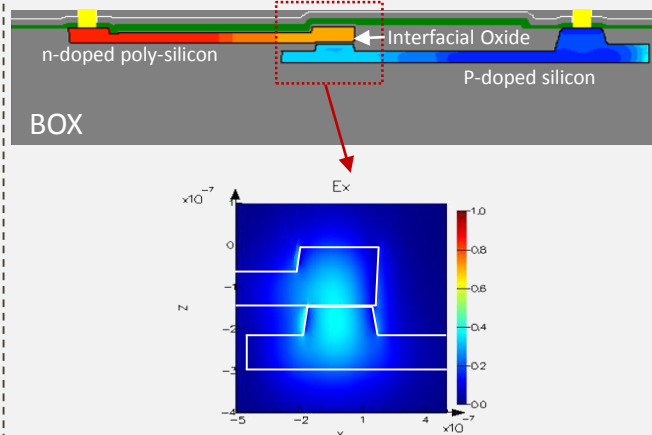
27

Capacitive structures substituting junctions

Vertical Interface



Horizontal Interface



Vertical Integration

1.6pF/mm capacitance oxide ([3;10]nm oxide thickness range)

1.2Vpp voltage swing ([0.6-1.8]V) with a DC bias to put swing around flat-band voltage and use accumulation charges

→ 1.52pJ/bit at 56Gb/s

Horizontal Integration

1.1pF/mm capacitance oxide ([5;15]nm oxide thickness range)

0.9Vpp voltage swing ([0.9-1.8]V) with a DC bias to put swing around flat-band voltage and use accumulation charges

→ 0.37 pJ/bit at 56Gb/s

Push-pull MZI with 30° phase shift on both branches:

→ Active Length <1mm

Summary & Conclusions

28

- New feature in CMOS: wafer size did not evolve for more than one and a half decade.
 - Traditionally, old tools were used for diversification (Ex: MEMS). It is not the case for silicon photonics.
 - Silicon photonics shares the same 300mm fab tools as other high-end technologies. Strict regulations about tool contamination or deviation.
 - Process evolution, new material introduction and device integration are all technically possible but not under any conditions.
 - Silicon photonics is a promising market and strategic efforts must be done to cover a wide variety of applications



leti



DEVICE & PROCESS



SILICON PHOTONICS



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THALES
UNIVERSITE PARIS-SUD
AIFOTEC FIBEROPTICS
NXP SEMICONDUCTORS
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UNIVERSITY OF SOUTHAMPTON, ORC
UNIVERSITY OF ST ANDREWS
FINISAR