OPTOELECTRONICS PACKAGING FOR EFFICIENT CHIP-TO-WAVEGUIDE COUPLING

G. VAN STEENBERGE, E. BOSMAN, J. MISSINNE, B. VAN HOE,

K.S. KAUR, S. KALATHIMEKKAD, N. TEIGELL BENEITEZ, A. ELMOGI

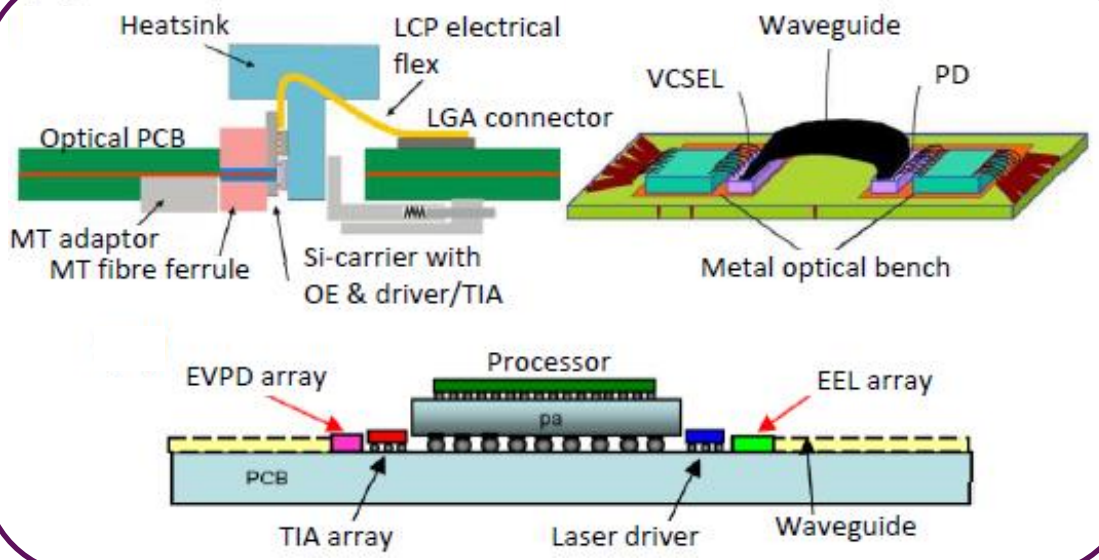
CONTACT GEERT.VANSTEENBERGE@ELIS.UGENT.BE

Cmst

UNIVERSITEIT GENT

imec

OPTOELECTRONICS PACKAGING

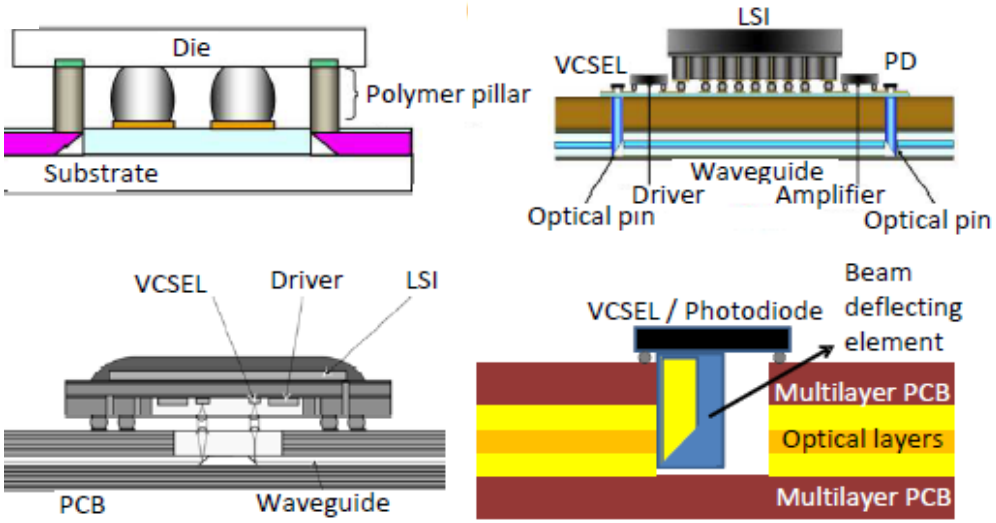


In-plane coupling approach schemes

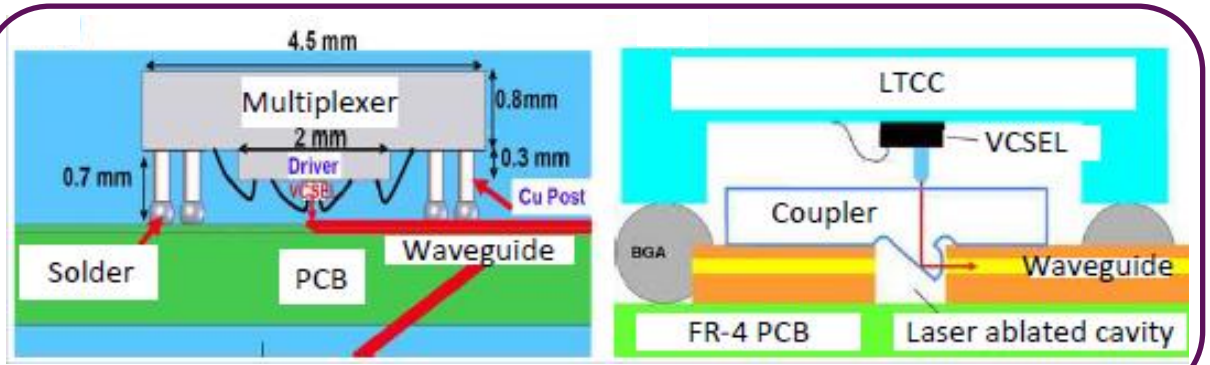
IBM, ETRI, Georgia Inst. of Technol.

Vertical light confinement between optoelectronics and waveguides

Fujitsu, Tokai Univ., NTT, Siemens C-LAB



OPTOELECTRONICS PACKAGING

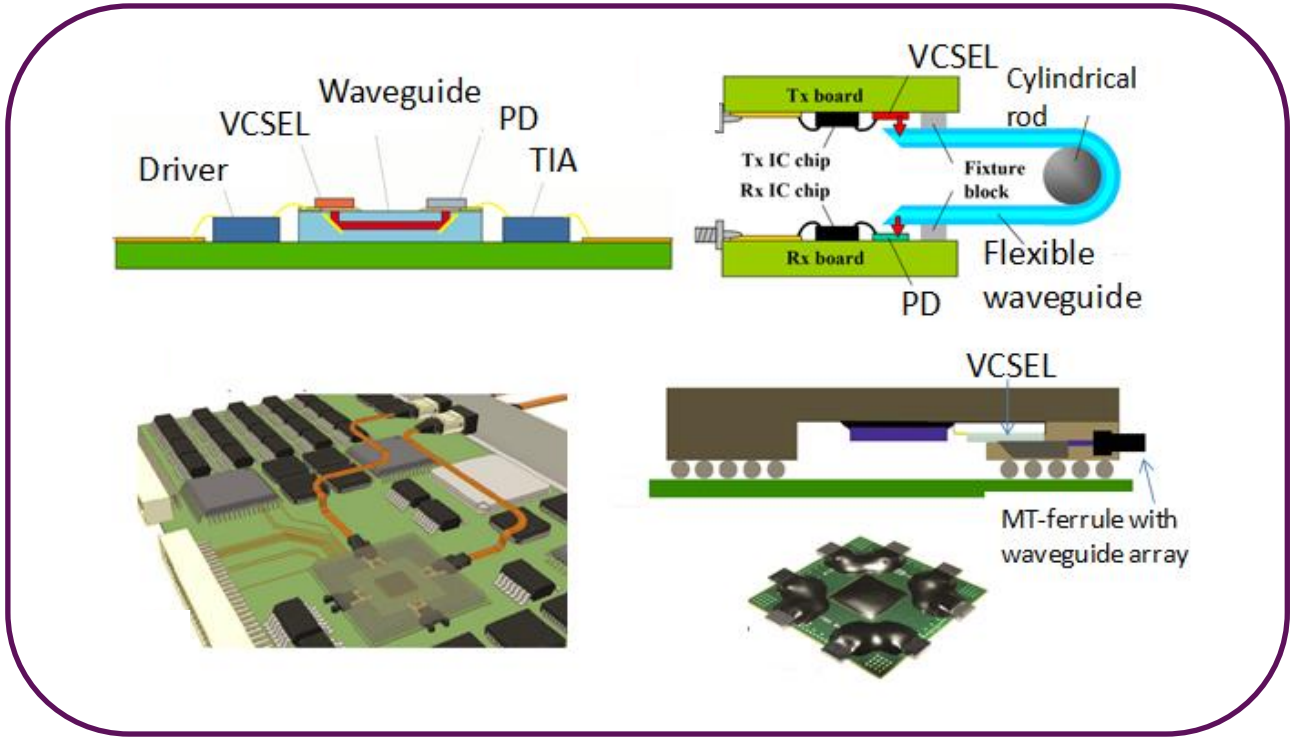


Vertical proximity coupling

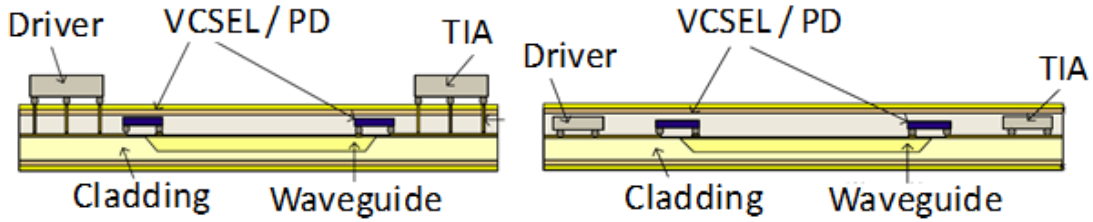
Institute of Microelectronics (Singapore), Univ. Oulu.

Separate waveguide PCB approach

Central Glass Co., Ltd. (Japan), Korea Photonics Technol. Inst., Reflexphotonics

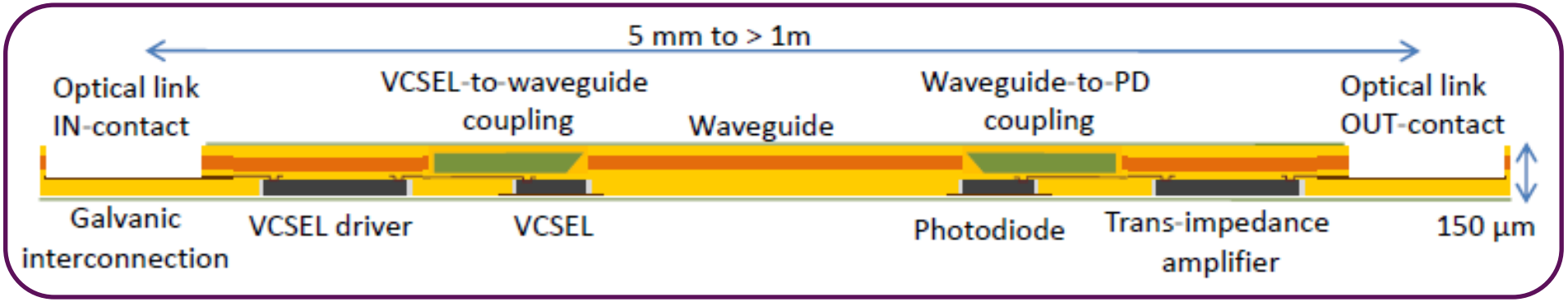


OPTOELECTRONICS PACKAGING



Embedding of optoelectronics in RCC laminates

Inha Univ. (South Korea)



Embedding of optoelectronics in flex substrates

Ghent Univ. / imec

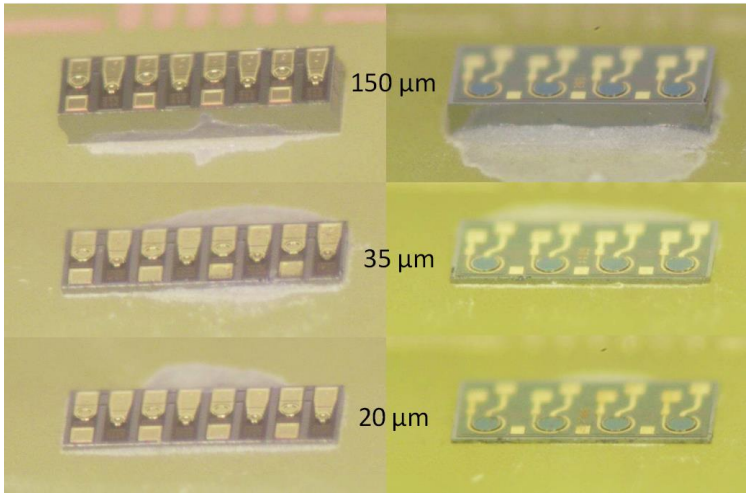
ULTRA-THIN OPTOELECTRONIC CHIP PACKAGE

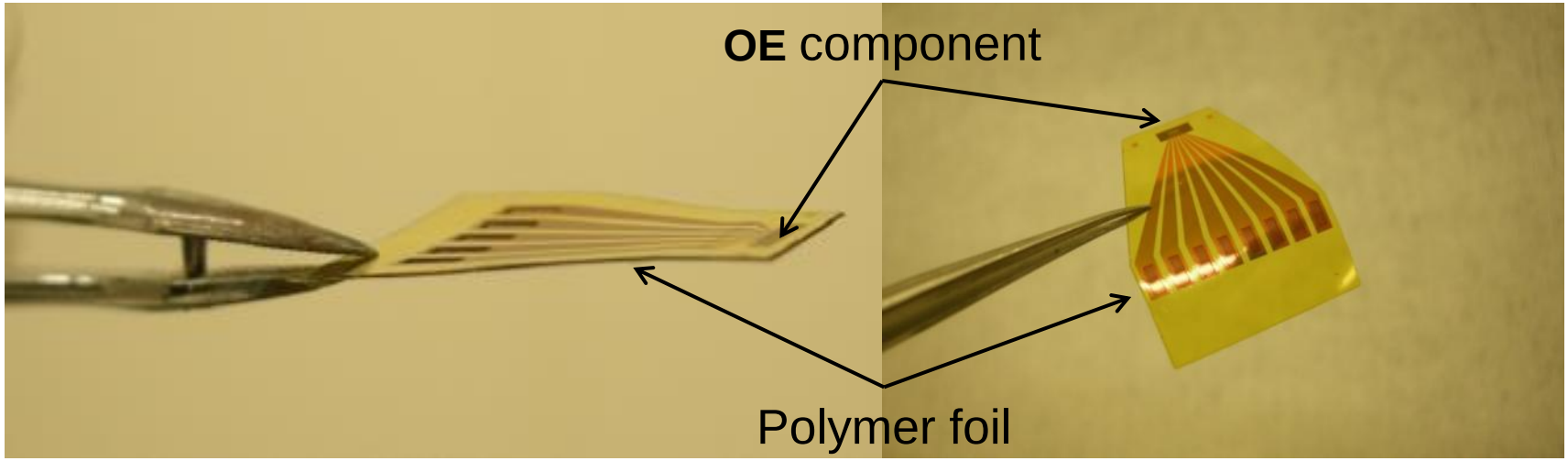
"Ultra thin optoelectronic package"

- Thinned commercial (opto)electronic components
- Embedded in **thin** & **flexible** polymer **foils**

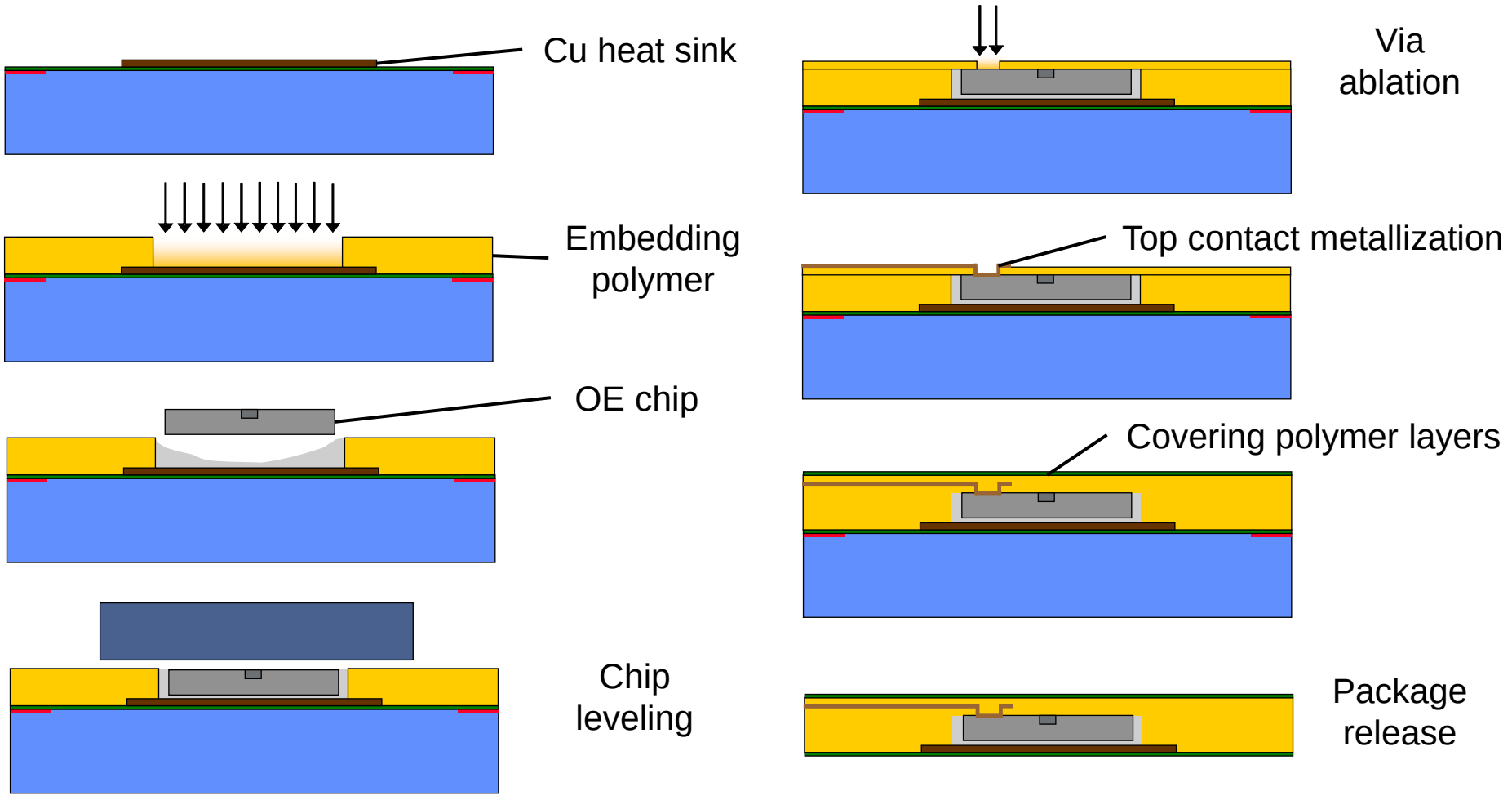
Component (bare die) thickness ~20µm

Total thickness ~40µm





ULTRA-THIN OPTOELECTRONIC CHIP PACKAGE

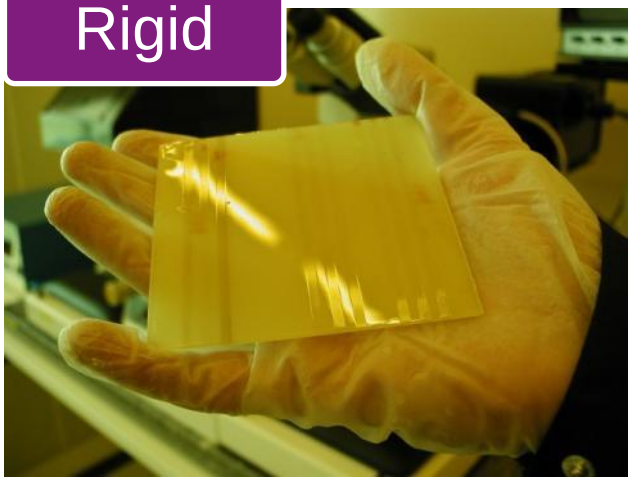


Precise process flow depends on substrate, polymer and component

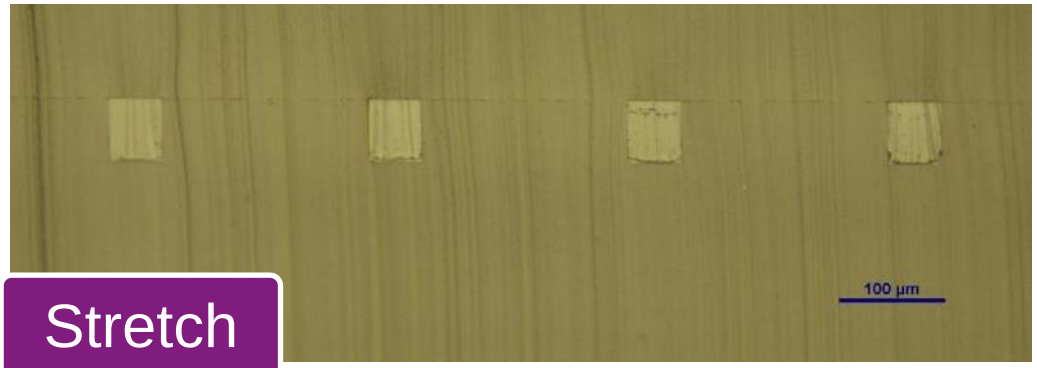
INTEGRATION WITH POLYMER OPTICAL WAVEGUIDES

- Acrylate, epoxy, silsesquioxanes, or silicone based
- Typical propagation loss below 0.1dB/cm

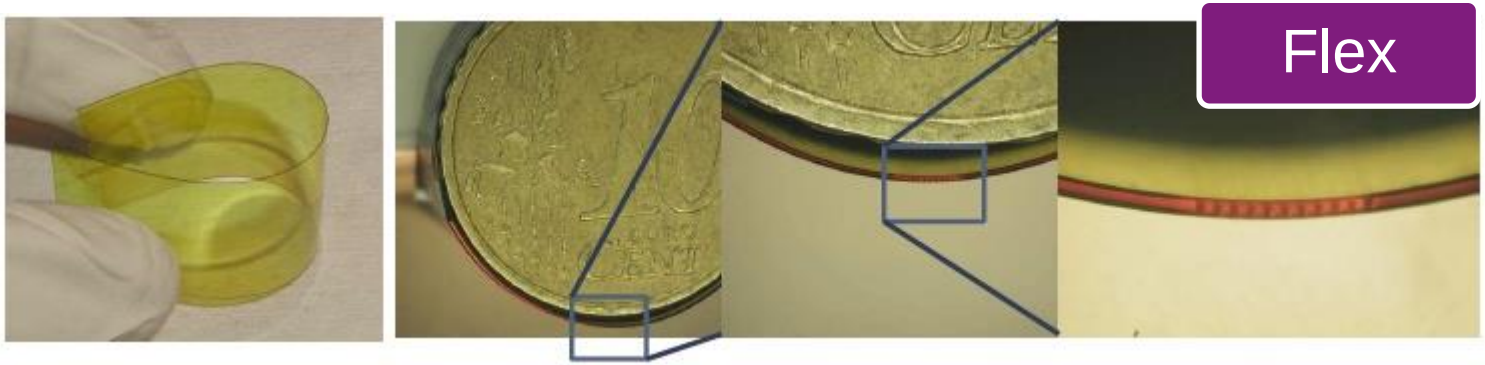
Rigid



Additional bending and stretching loss



Stretch

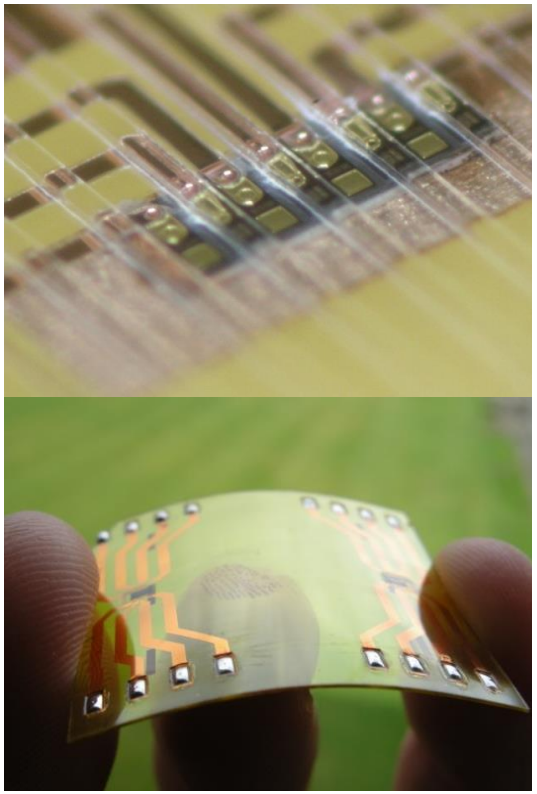


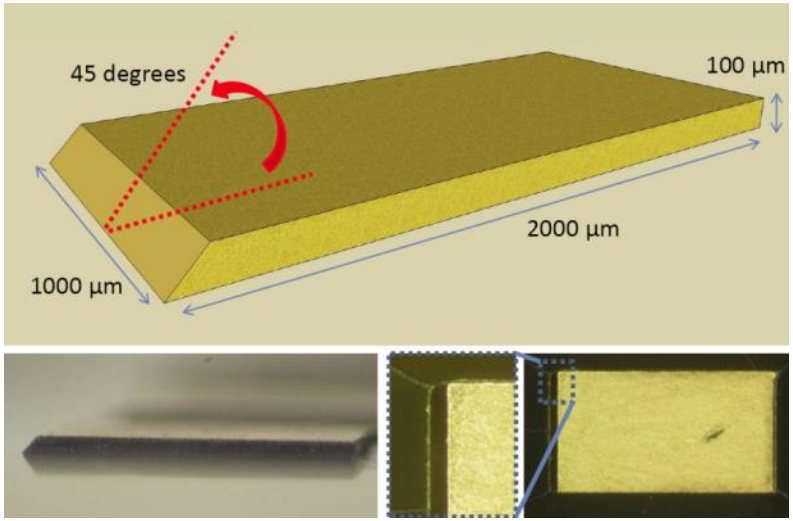
Flex

INTEGRATION WITH POLYMER OPTICAL WAVEGUIDES

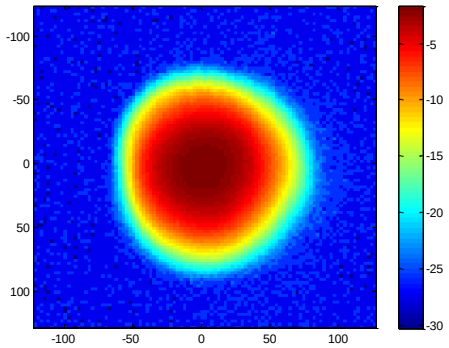
Sequential build-up approach

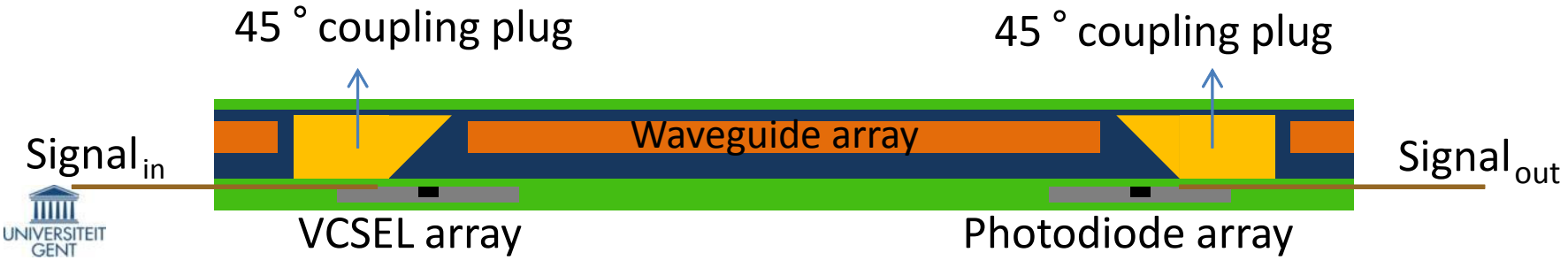
- Typical total optical loss 6dB





Mirror loss 0.5 dB



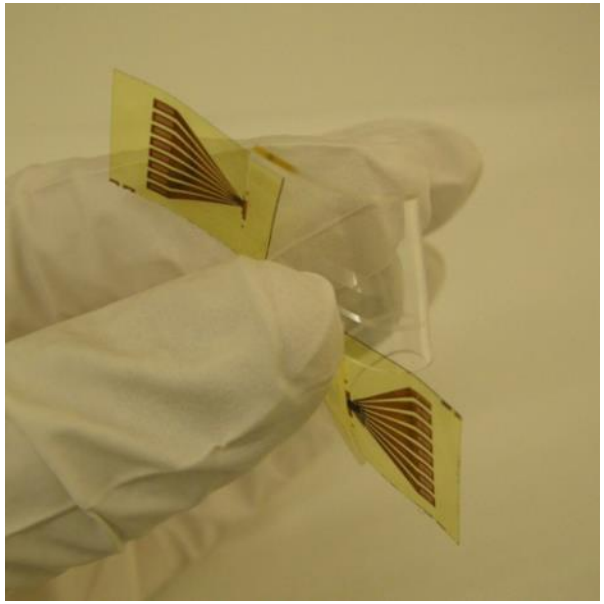


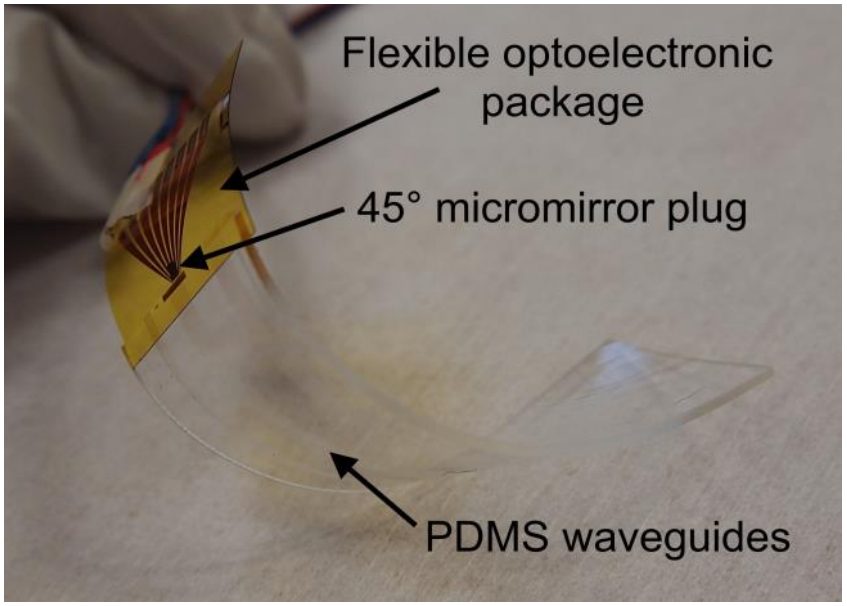
INTEGRATION WITH POLYMER OPTICAL WAVEGUIDES

Modular approach

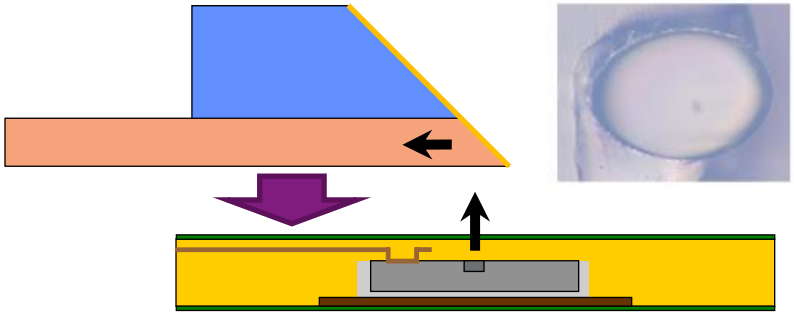
- Typical total optical loss 3dB

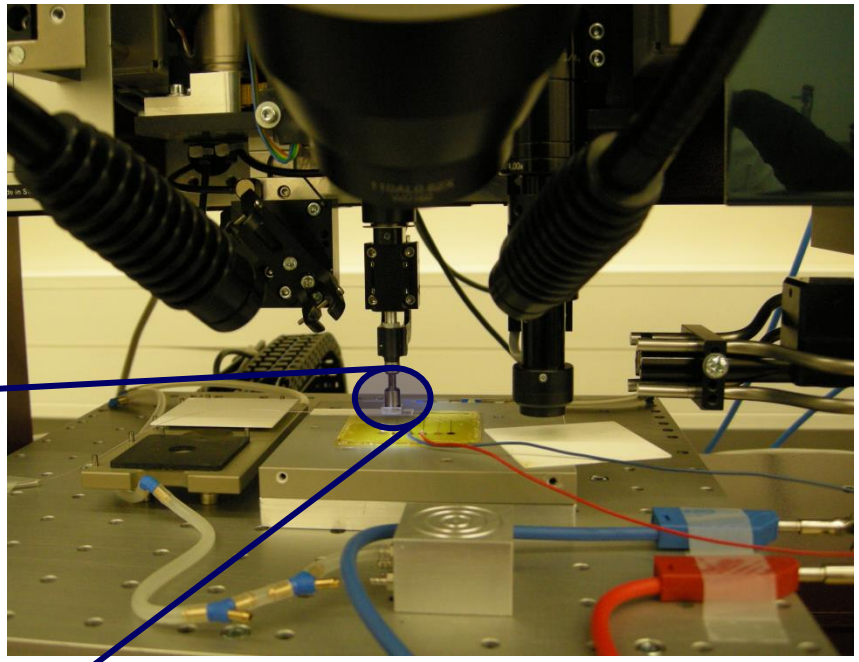
Stretching up to 30% without significant loss

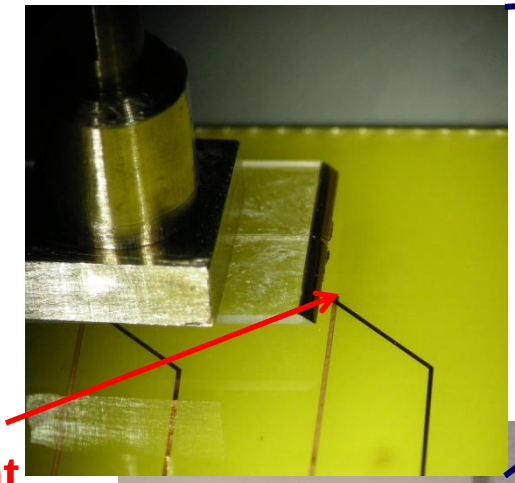




INTEGRATION WITH OPTICAL FIBERS

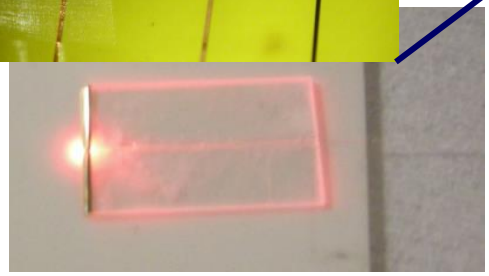


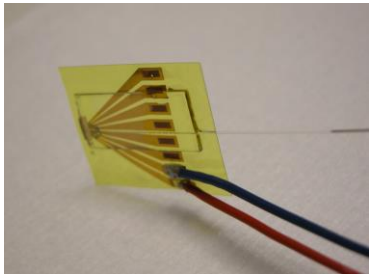


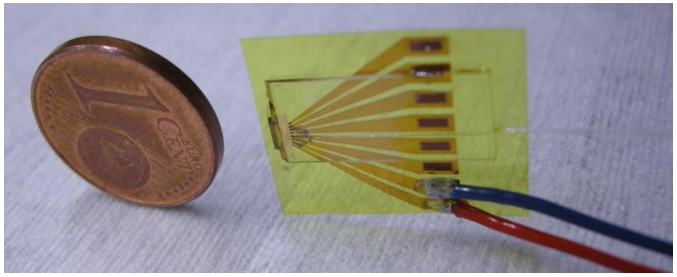


assembly based on
adapted flip chip process

OE component







Cmst

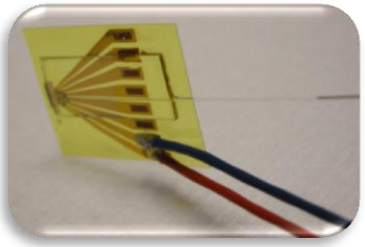
UNIVERSITEIT GENT

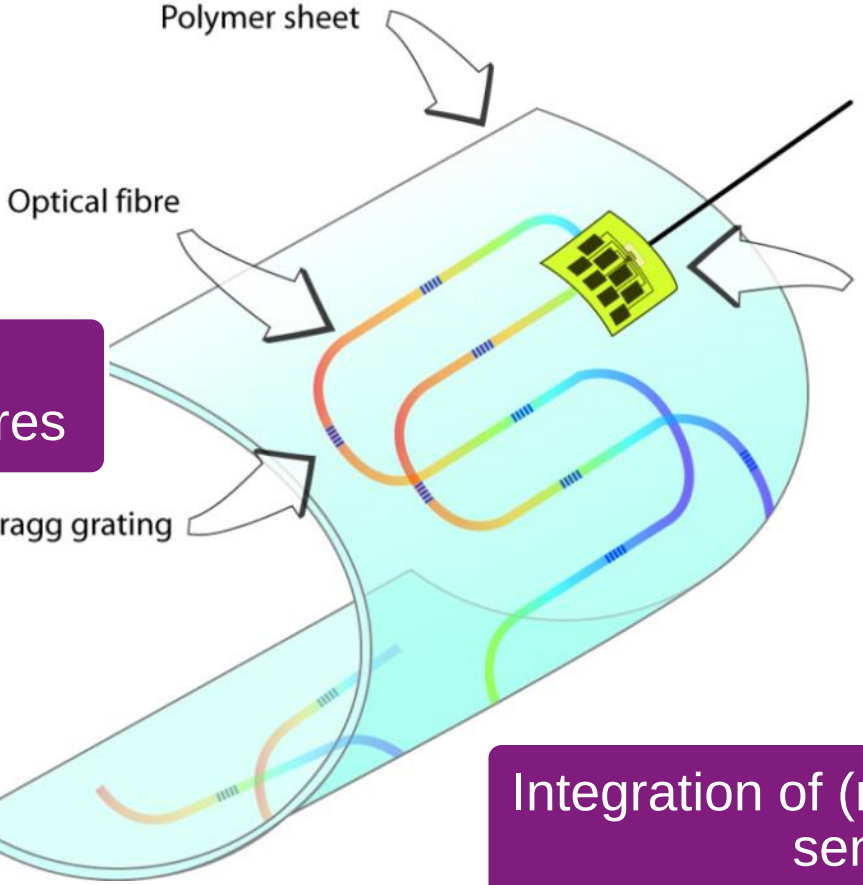
imec

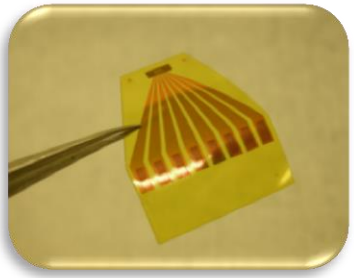
EU PROJECT PHOSFOS
PHOTONIC SKINS FOR OPTICAL SENSING

PHOSFOS
Photonic Skins For Optical Sensing

Integration of optoelectronic chips







Integration of coupling structures

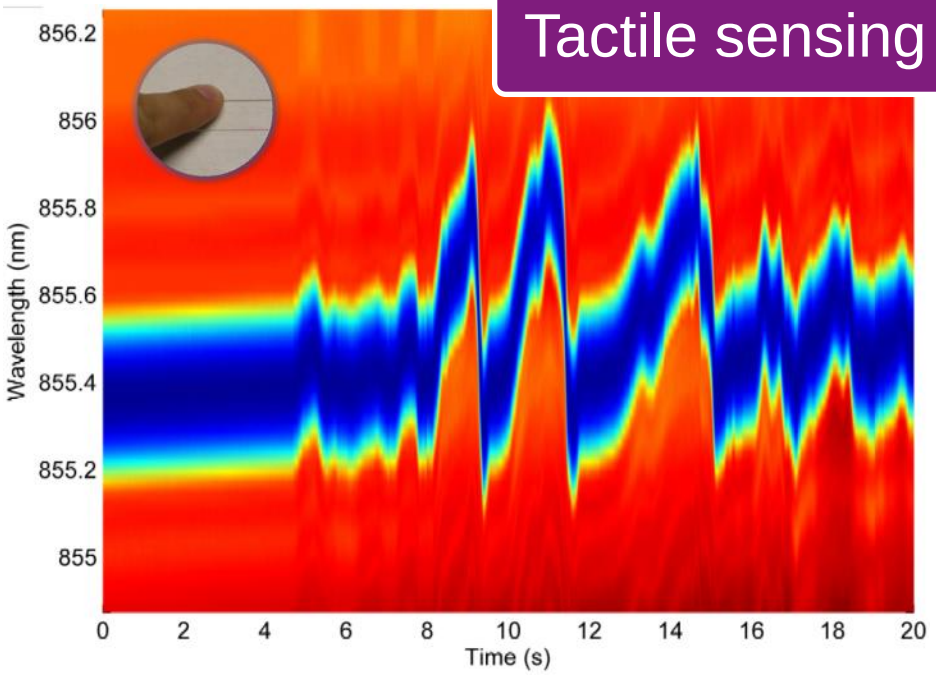
Integration of (multiplexed) fiber sensors

Cmst
UNIVERSITEIT GENT
imec

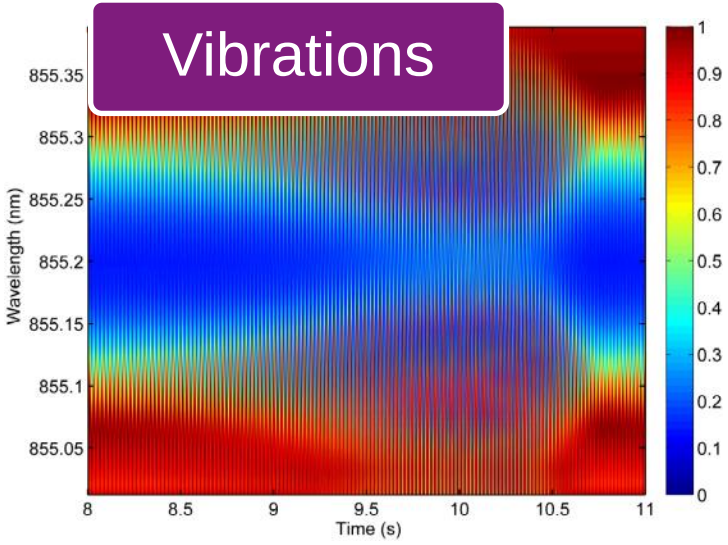
EU PROJECT PHOSFOS
PHOTONIC SKINS FOR OPTICAL SENSING

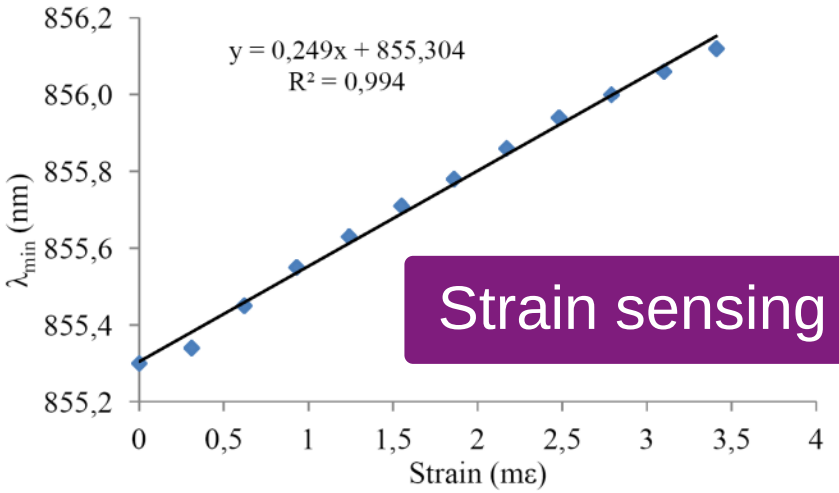
PHOSFOS
Photonic Skins For Optical Sensing

Tactile sensing



Vibrations





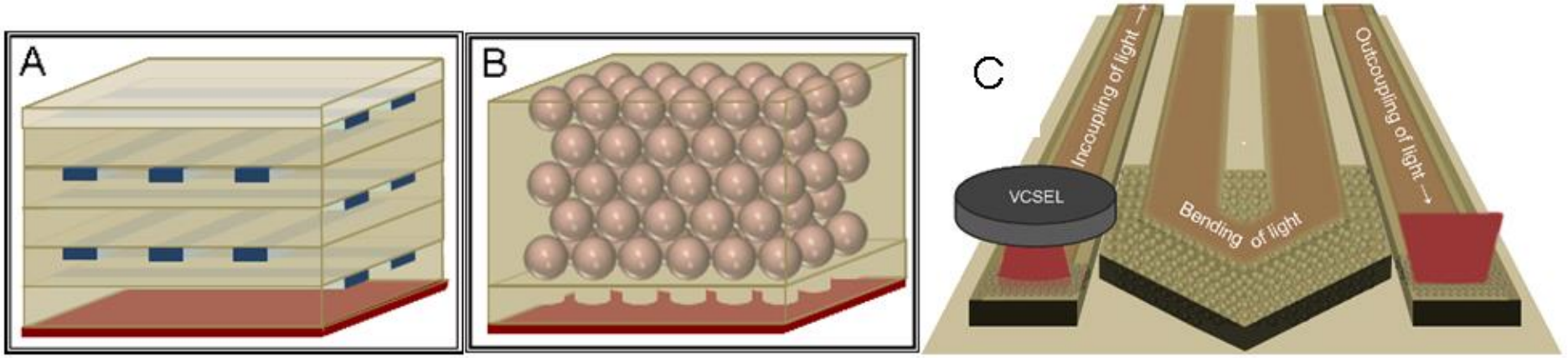
Strain sensing

Cmst
UNIVERSITEIT GENT
imec

EU PROJECT FIREFLY
MULTILAYER PHOTONIC CIRCUITS

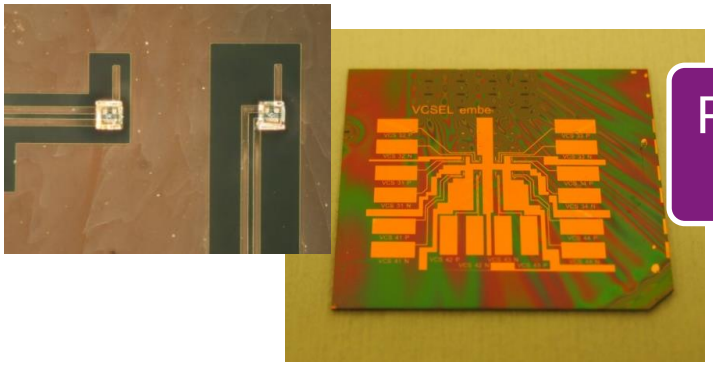
Challenges

- Integration of waveguides and VCSELs
- Integration of waveguides and glass fibers
- Integration of photonic crystals and waveguides



Multilayer Photonic Circuits made by Nano-Imprinting of Waveguides and Photonic Crystals

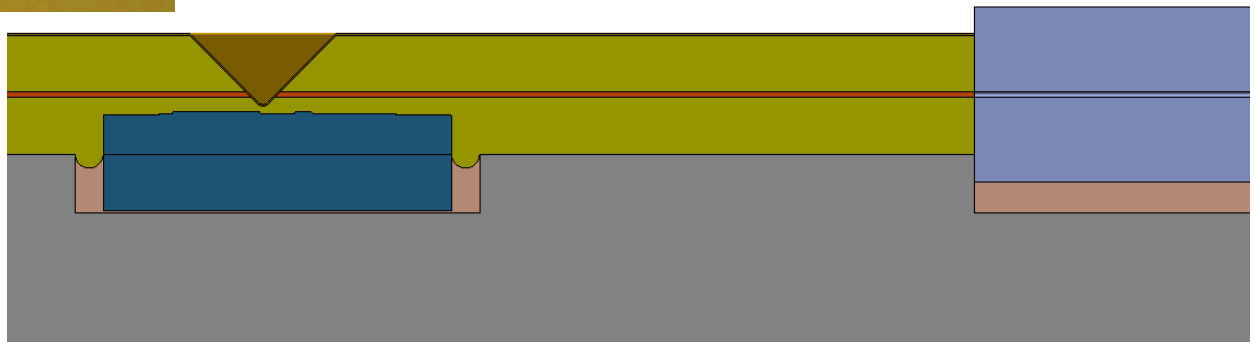
EU PROJECT FIREFLY
VCSEL – WAVEGUIDE INTEGRATION

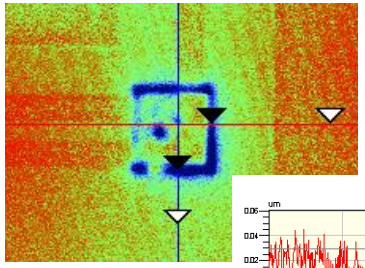


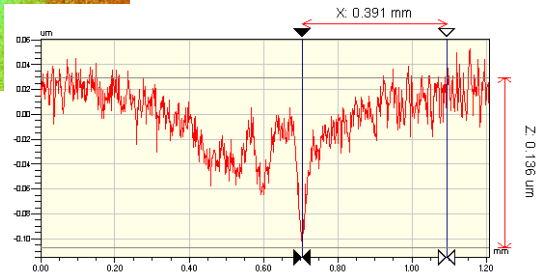
Face-up embedding of VCSELS

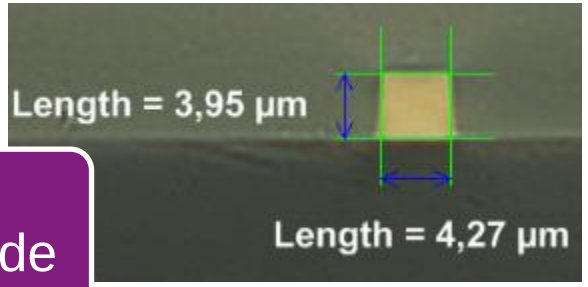
FIREFLY

Planarity after chip embedding









Single mode polymer waveguide technology

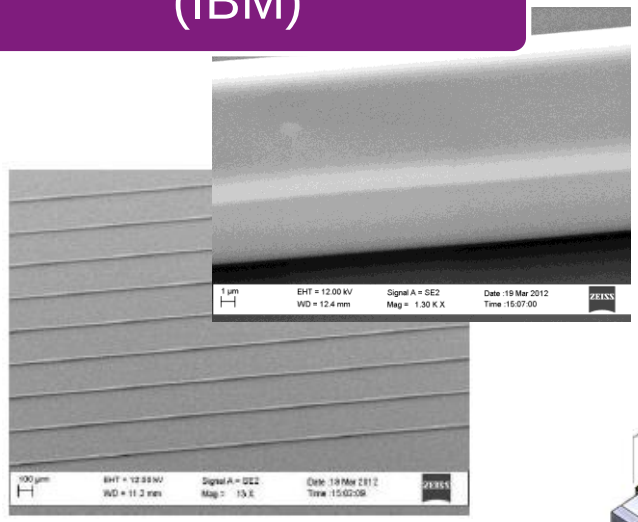
Cmst

UNIVERSITEIT GENT

imec

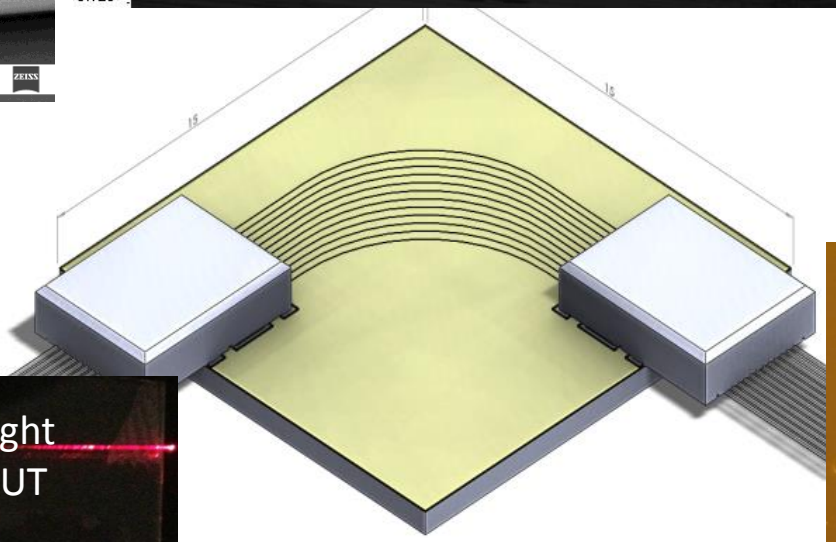
EU PROJECT FIREFLY
WAVEGUIDE – FIBER INTEGRATION

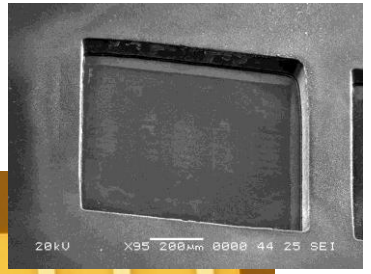
Laser direct writing (IBM)

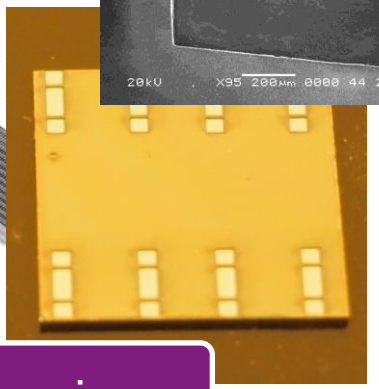


End facet (TE Connectivity)

FIREFLY







Initial testing (TE Connectivity)

Laser cleaning

Cmst

UNIVERSITEIT GENT

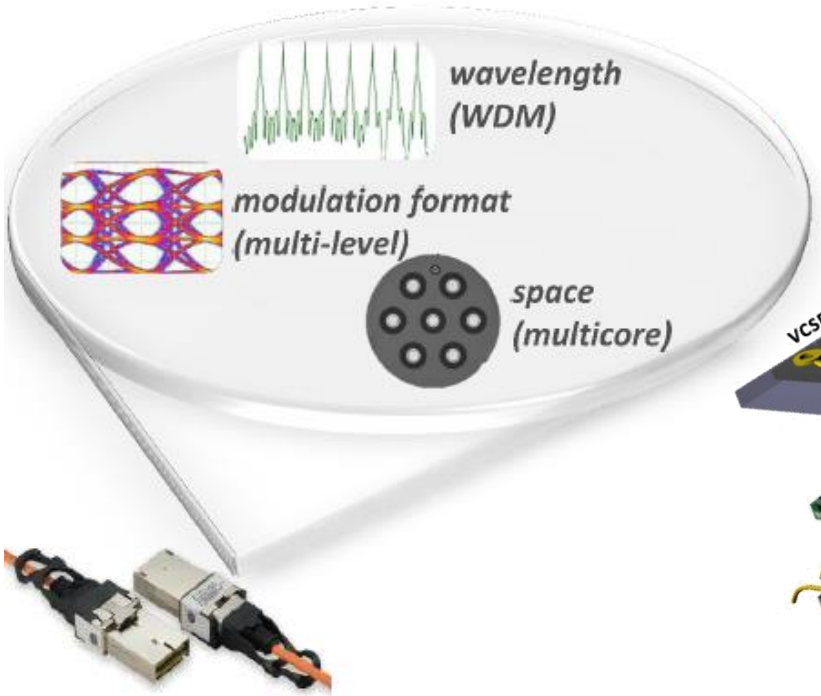
imec

EU PROJECT MIRAGE
TERABIT CAPACITY AOC

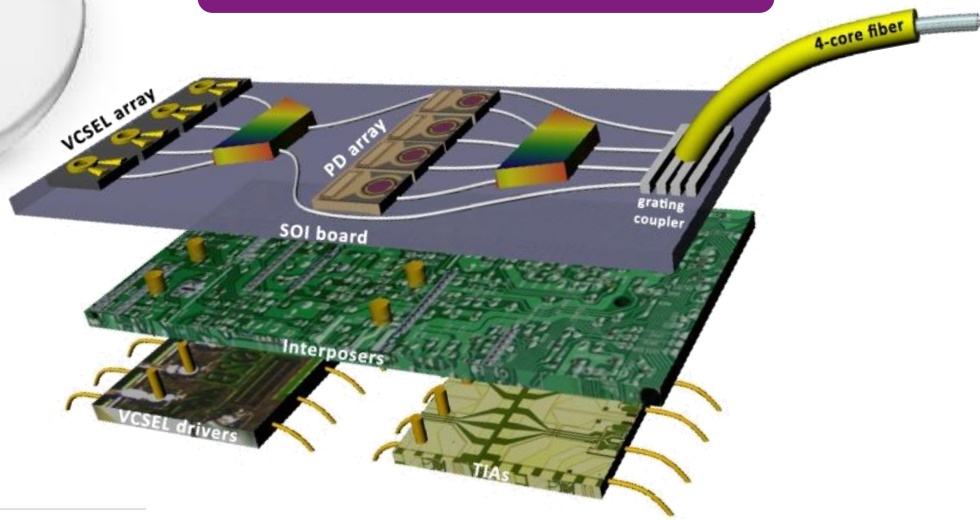
Scale line rate to 40G

Introduce new degrees of parallelization

- WDM | multi-core | multi-level



3D photonic-electronic integration

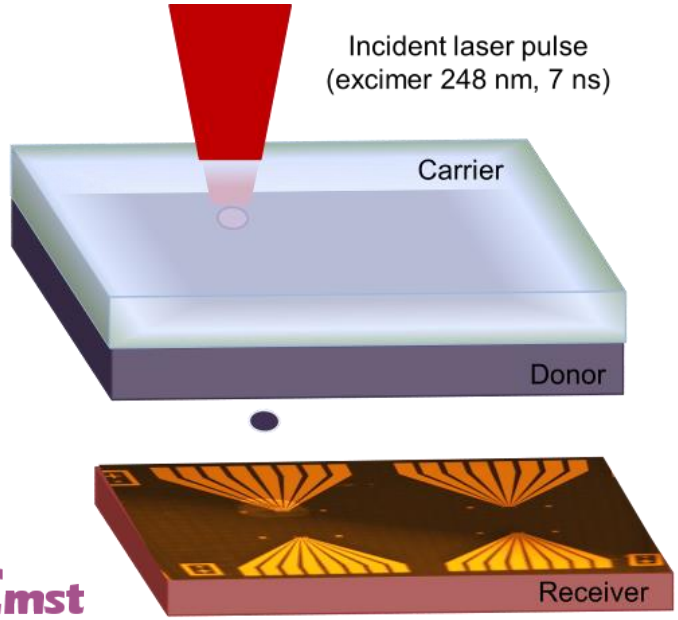


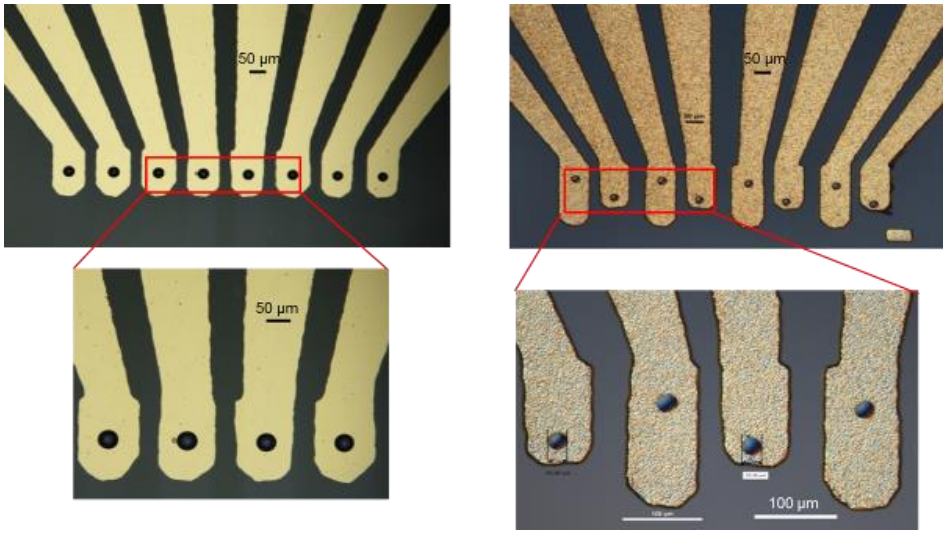
EU PROJECT MIRAGE
TERABIT CAPACITY AOC

Optoelectronics assembly

- Accurately defining micro-bumps using

1 “Laser Induced Forward Transfer” (LIFT)





Adhesive bonding / thermocompression

EU PROJECT MIRAGE
TERABIT CAPACITY AOC

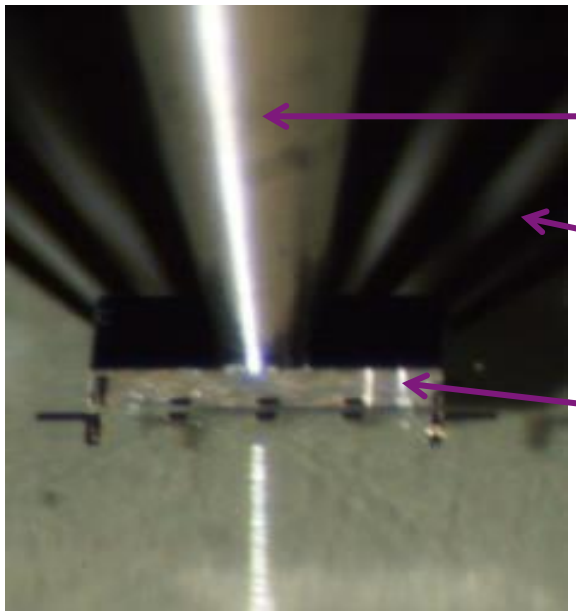
Optoelectronics assembly

- Flip chip bonding of the die

2

= chip placement + adhesive curing

+ thermo-compression bonding

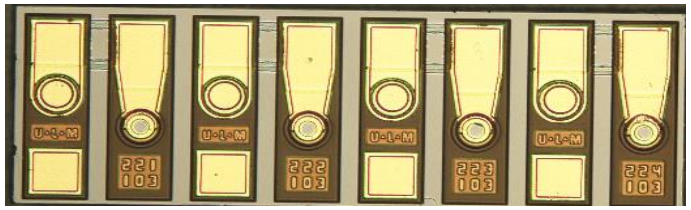


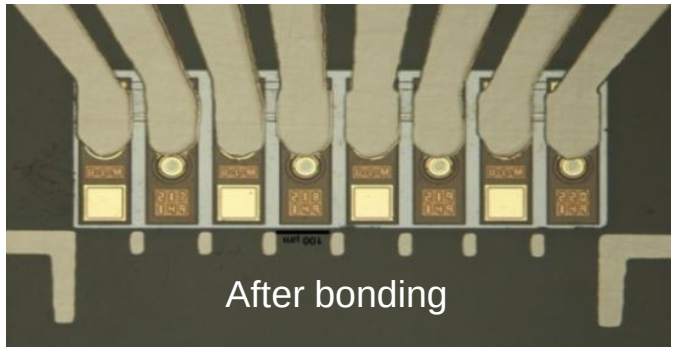
Flip chip bonder chuck

Substrate + metal tracks + adhesive bumps

OE chip (active area facing down)

VCSEL test chip (1x4 array)





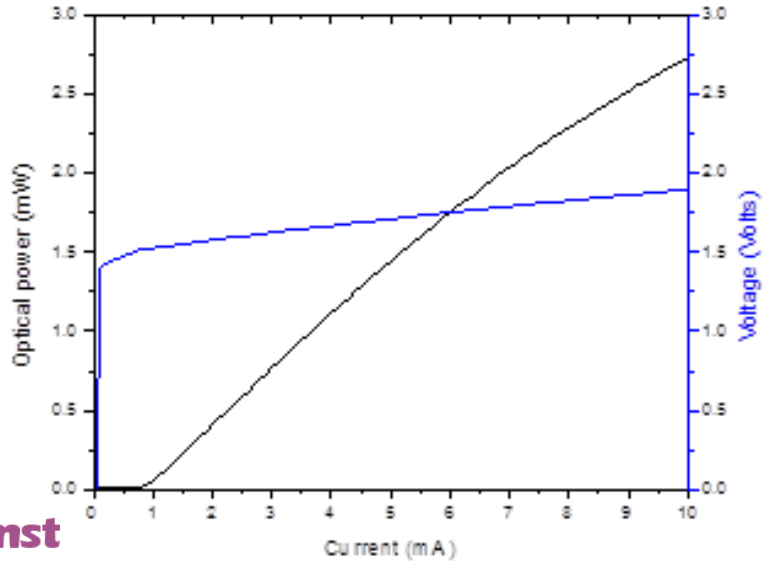
EU PROJECT MIRAGE
TERABIT CAPACITY AOC

Optoelectronics assembly

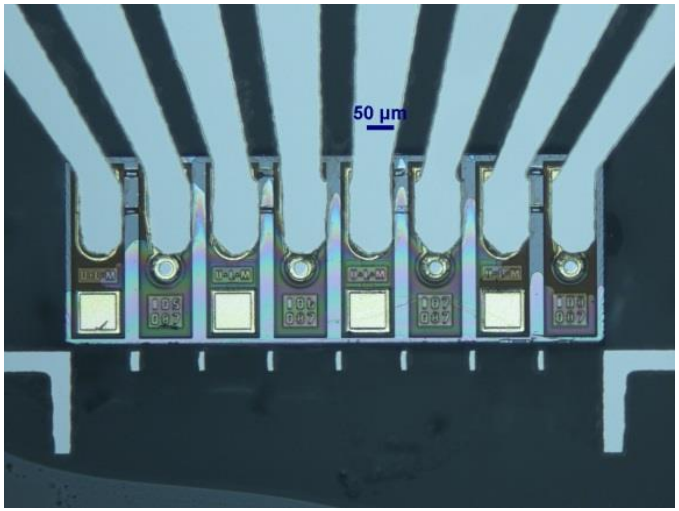
- Characterization of bonded VCSEL/PD chips
- Shear testing after bonding

3

LVI curve for bonded test VCSELs

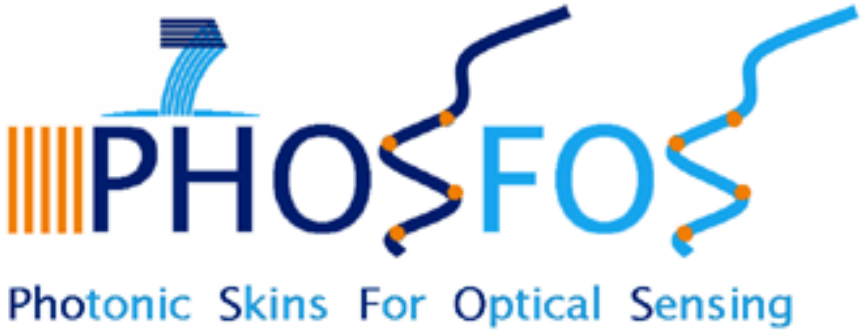


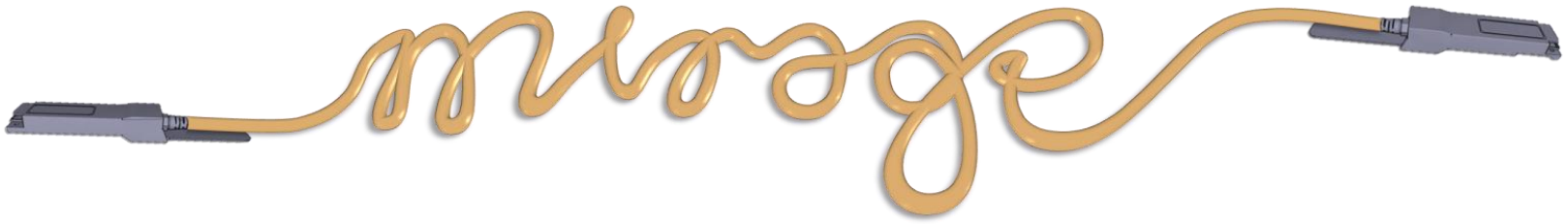
chip encapsulation



ACKNOWLEDGEMENT

FIREFLY





Cmst

UNIVERSITEIT GENT

imec

THANK YOU

Cmst

UNIVERSITEIT GENT

imec