

Overview and Roadmap for European projects in Optical Interconnects

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<http://phos-net.csd.auth.gr/>

CERTH
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RESEARCH & TECHNOLOGY
HELLOS
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THE CENTRE FOR

Why is an overview needed ?

- *To identify possible synergies*
- *To understand the strategy of the EC R&D*
- *To identify possible “blank” or “uncovered” areas*
- *...and orchestrate all this into a coherent strategy with the final aim being:*
 - *a stronger European industry on OI*
 - *a stronger European R&D on OI*
 - *a more intense industry-academia collaboration*

Some history



POLYSYS

On-board interconnects
polymer+InP
STReP, ~2.5M



Optical RAM
SOI+III-V
FET-STReP, ~2M

~11.7M



On-chip interconnects
SOI+plasmonics
STReP, ~7.3M



On-board interconnects
polymer+PhCrystals
STReP, ~3.4M

~8M



PhoxTroT

Photonics for High-Performance, Low-Cost & Low-Energy Data Centers, High Performance Computing Systems, Terabit/s Optical Interconnect Technologies for On-Board, Board-to-Board, Rack-to-Rack data links

All hierarchy levels
SOI+III-V+polymer
+glass+plasmonics+IC
IP, ~8.7M

HISTERIC

Optical digital logic
InP-on-SOI +PhC
STReP, ~2.3M



Chip-to-Chip
plasmonics
STReP, ~2.4M



Active Optical Cable
III-V+SOI+multicore
STReP, ~3M

2010

2011

2012

Source: http://cordis.europa.eu/fp7/ict/photronics/projects-fp7_en.html

Nikos Pleros

Some conclusions

❖ **Increasing interest between 2010-2012**

❖ *FP7 funding on OI projects increased from 7.3 to 11.7MEuro*

❖ **Total EU contribution ~27 M€**

❖ *3 projects funded under **Obj. “Disruptive Photonic Technologies”***

❖ *1 project funded under **FET Open***

❖ *Only 4 projects funded under **Obj. “Photonic Components”***

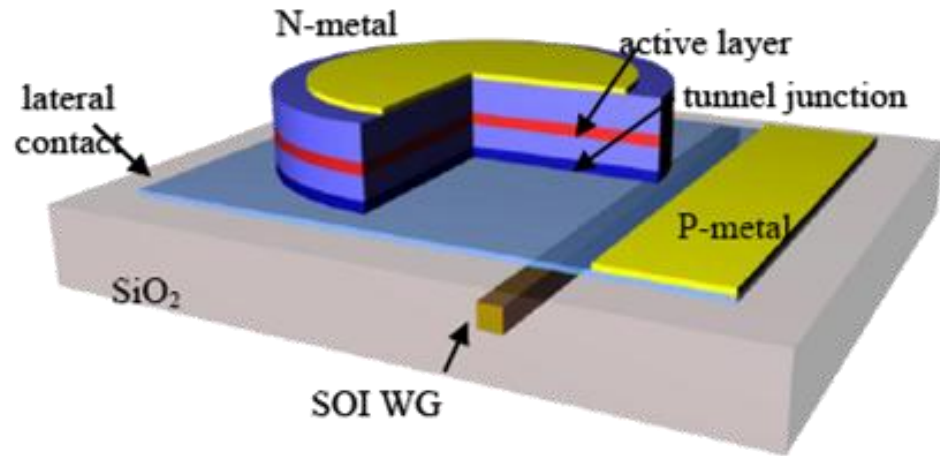
**non-focused CfP,
random approach**

...and some technology

<http://www.ict-historic.eu/>



coordinated by
IMEC, Belgium



Heterogeneously integrated microdisk lasers on SOI.

(L. Liu et al, Nature Photonics, Jan 2010, DOI: 10.1038/NPHOTON.2009.268)

- ✓ InP + SOI + PhC
- ✓ goal: flip-flops and digital circuits
- ✓ demonstrated low-energy, ultra-small, high-speed FFs

coordinated by ICCS/NTUA, Greece



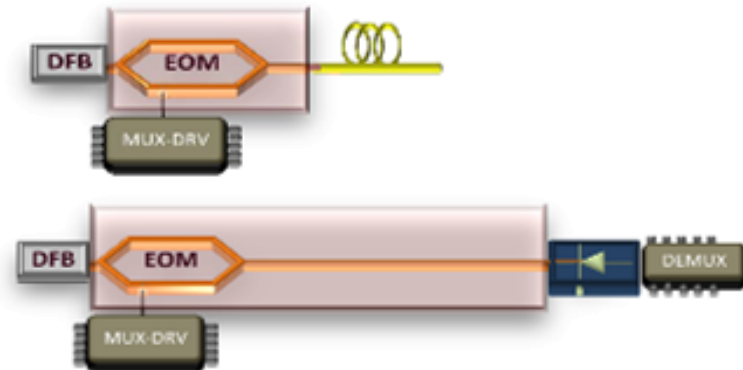
Serial 100 Gb/s optical transmission based on:

EO polymers for high-speed modulation

InP for high-speed photodetection

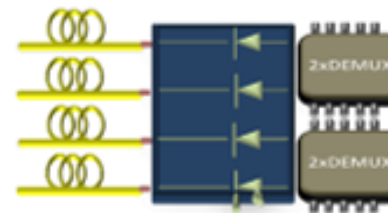
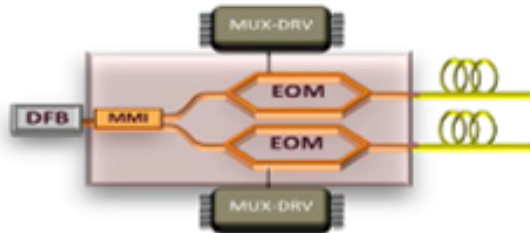
InP-DHBT for high-speed electronics

Hybrid integration, assembly, packaging



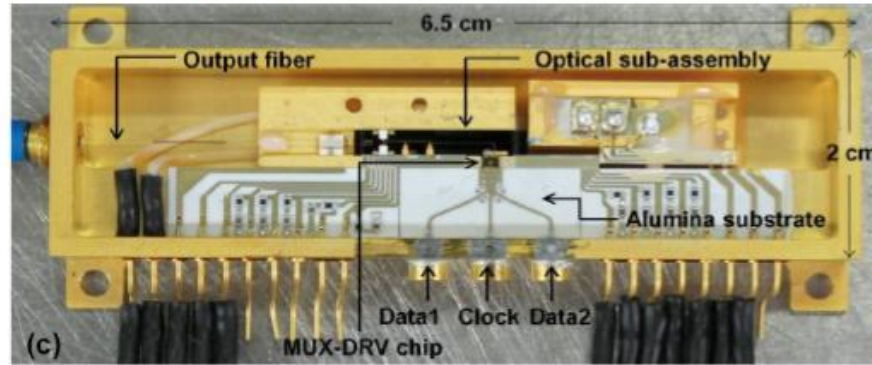
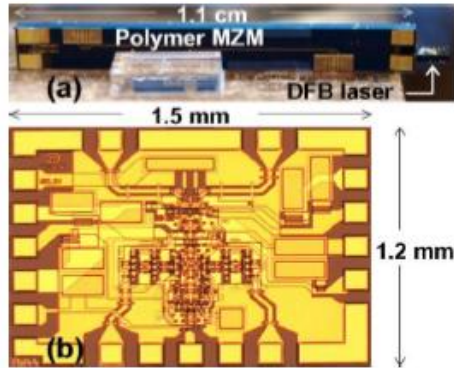
Scale the technology to higher capacity using arrayed components

2x 100 Gb/s and 4x100 Gb/s systems

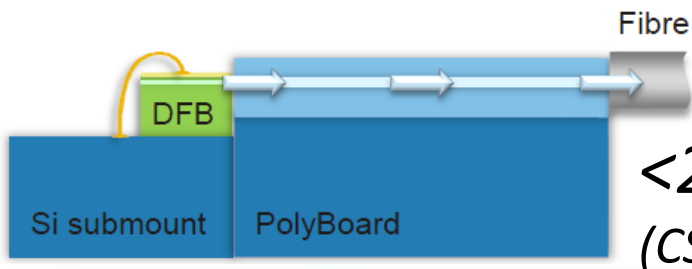


Applications in Telecom, Datacom and Computercom

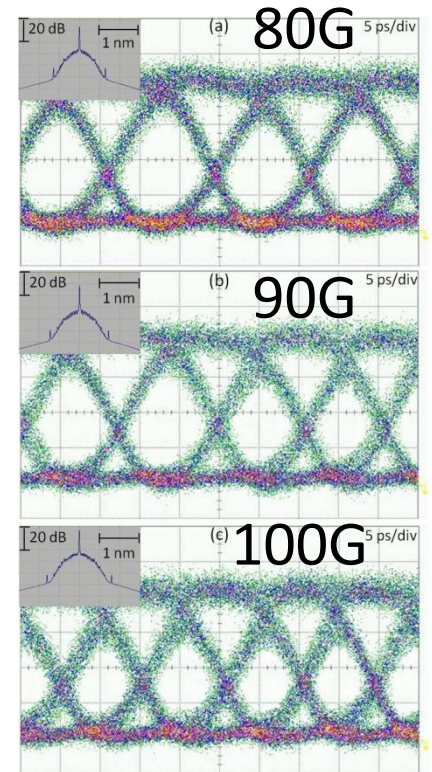
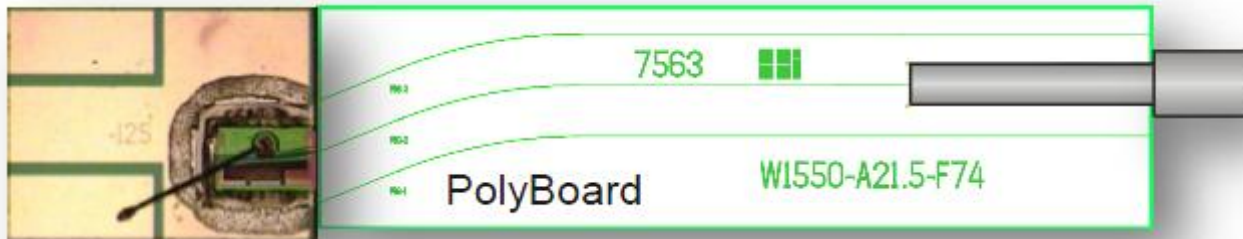
Serial 100 Gb/s NRZ-OOK connectivity, ~ 80 mW/Gb/s



(V. Katopodis et al, ECOC2012, PDP Th3.B.4)



< 2 dB coupling loss
 (CSDFB+PolyBoard+SMF)



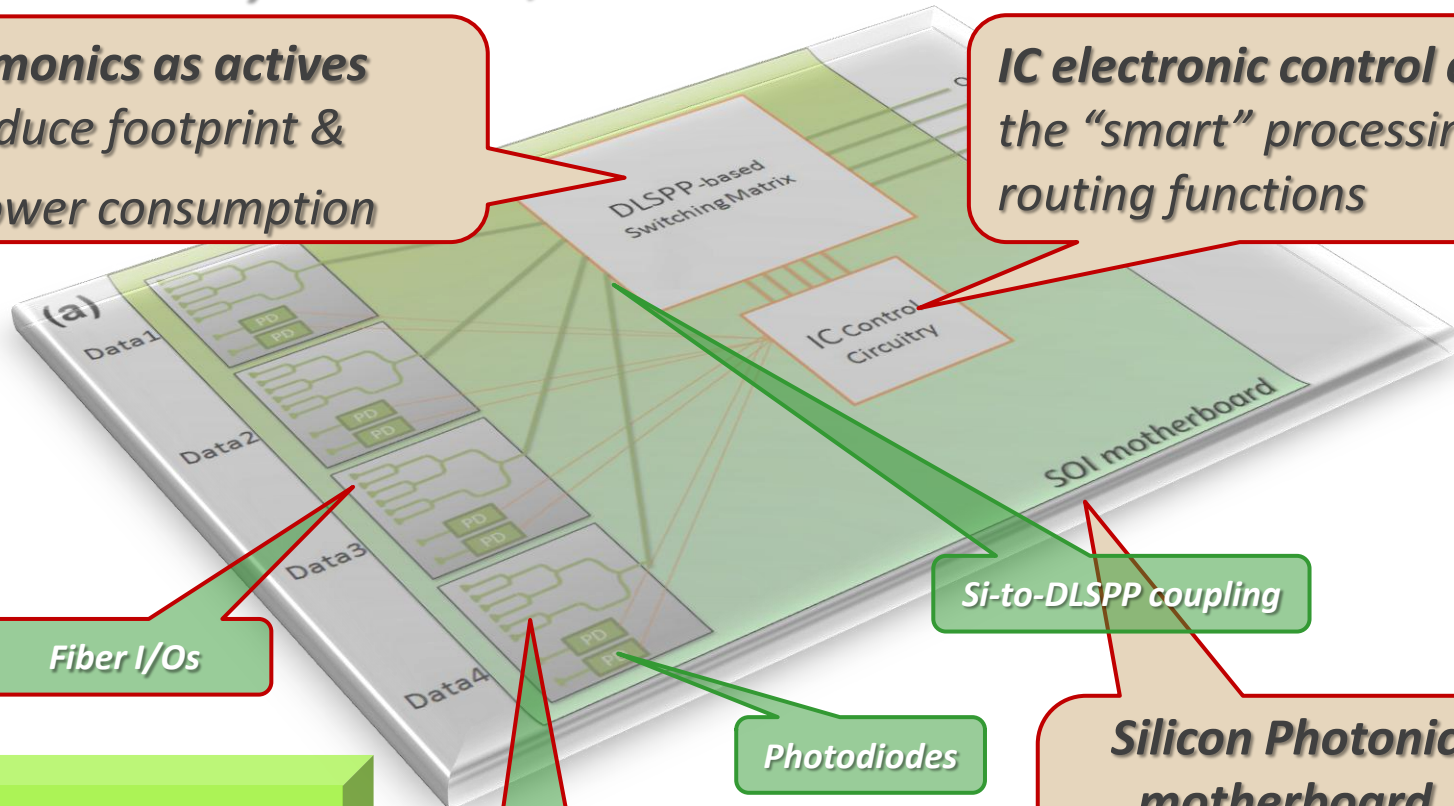
coordinated by CERN, Greece



Plasmonics as actives

- ✓ reduce footprint &
- ✓ power consumption

IC electronic control circuit
the "smart" processing and routing functions



Fiber I/Os

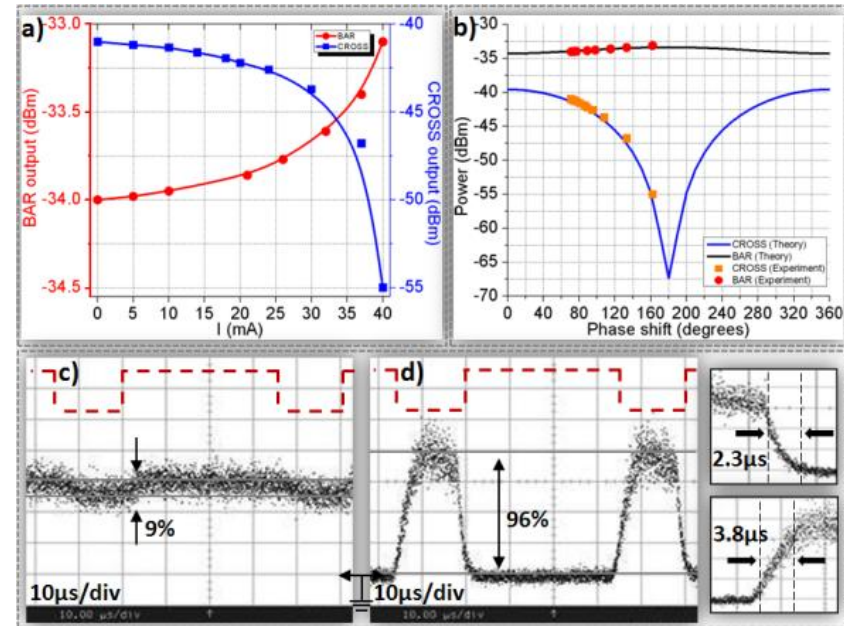
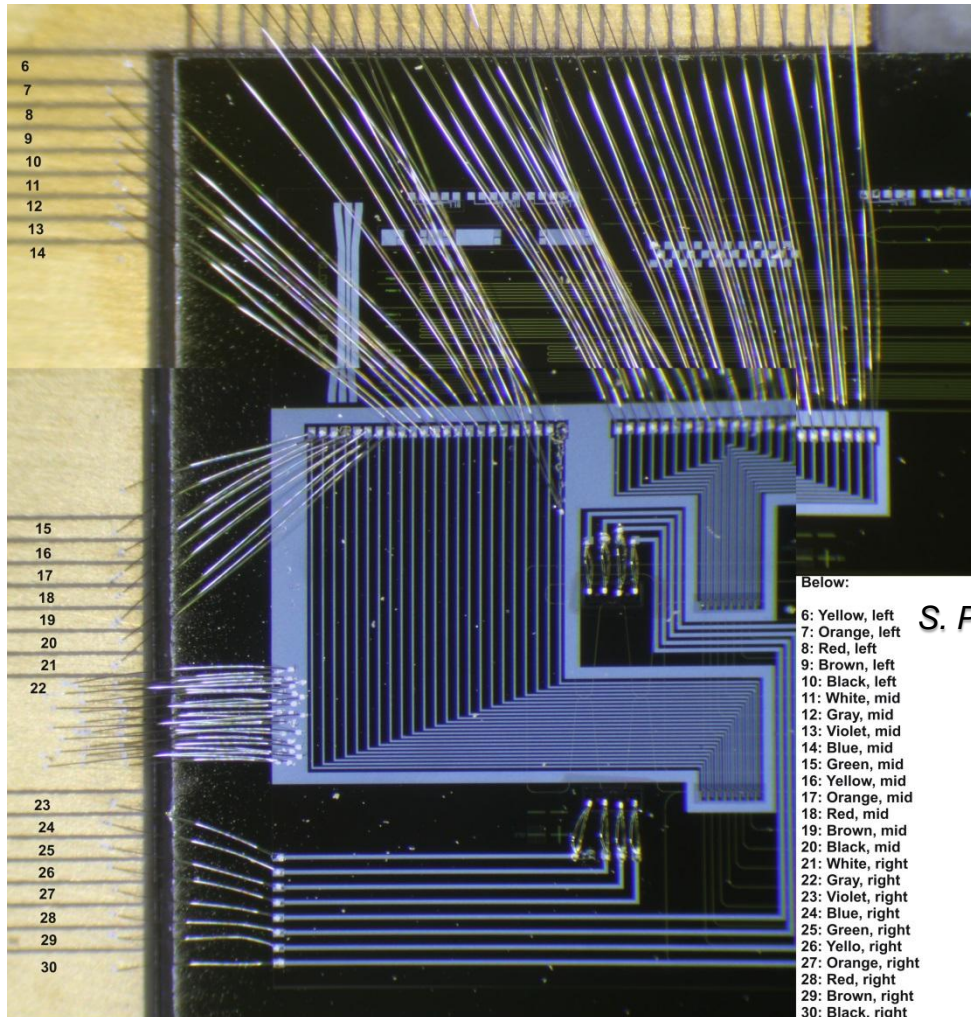
Si-to-DLSP coupling

Photodiodes

SOI multiplexer

**Silicon-Plasmonic
Network-On-Chip**

**Silicon Photonic
motherboard**
low loss technology
hosting platform

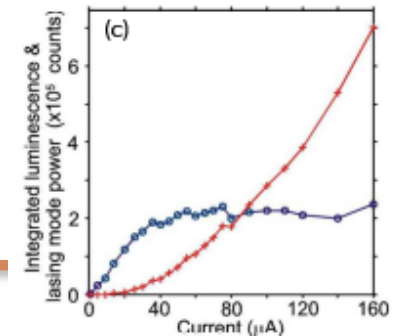
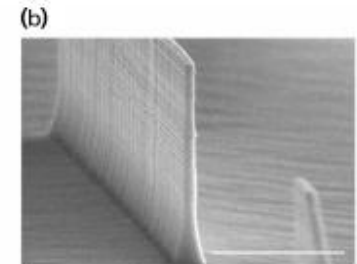
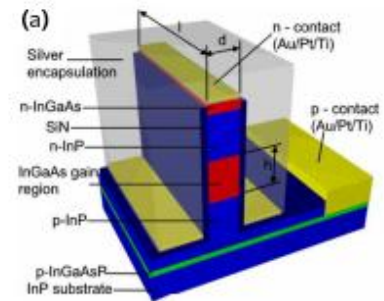
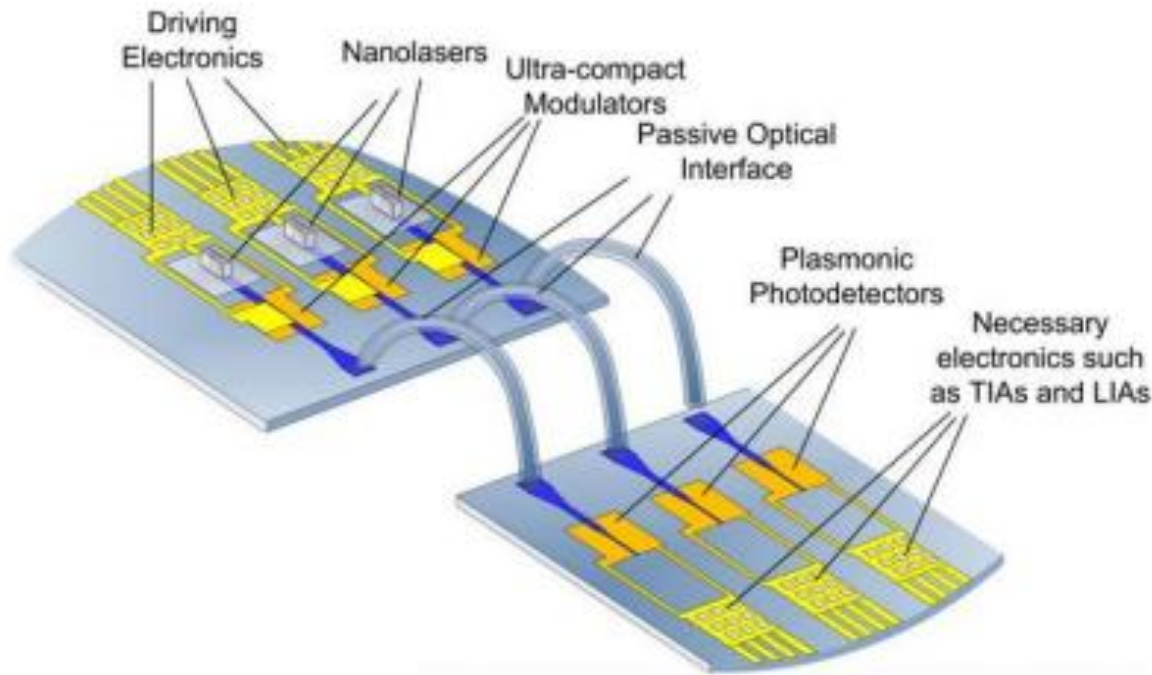


S. Papaioannou et al., *Nature Sci. Rep.* Article number: 652(2012)

- ✓ 3.8 μ s response
- ✓ 13.1mW power cons.
- ✓ 40Gb/s throughput
- ✓ Lowest P_{xt} value

coordinated by KIT, Germany

CMOS Chip-to-Chip interconnect





<http://www.fp7-firefly.eu>

FIREFLY

Multilayer Photonic Circuits made by Nano-Imprinting of Waveguides and Photonic Crystals

TNO

 **Tyndall**
National Institute
Institut National

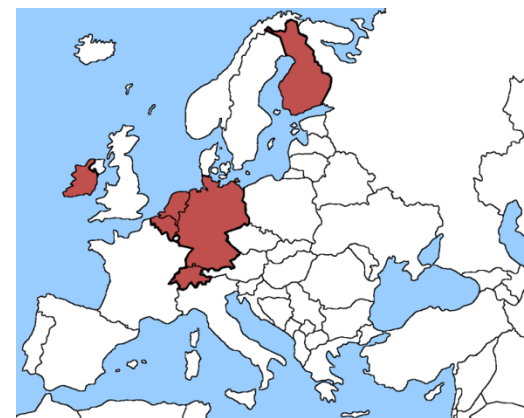
 **TE**
connectivity

 **imec**

IBM



Universiteit Utrecht

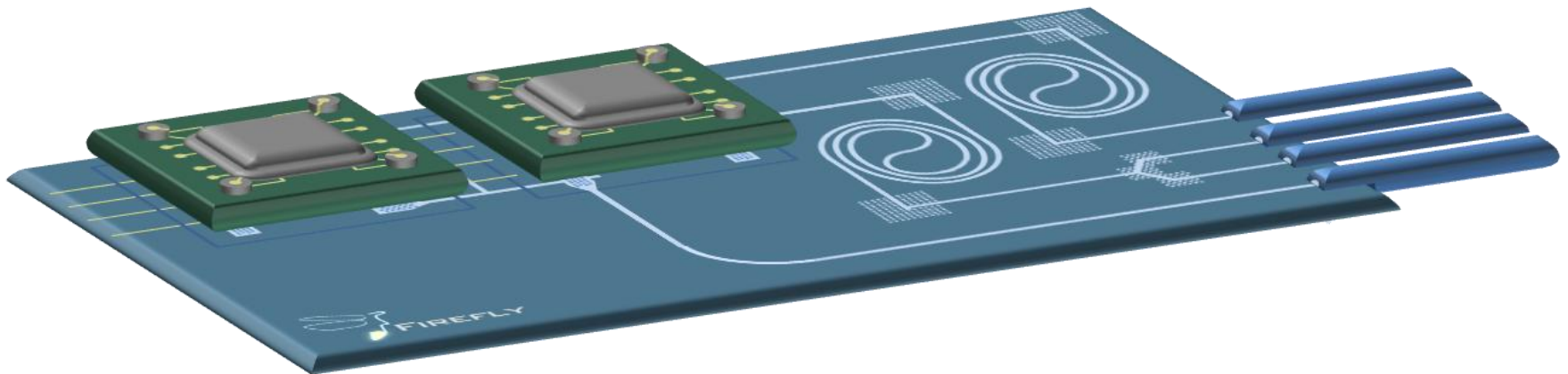


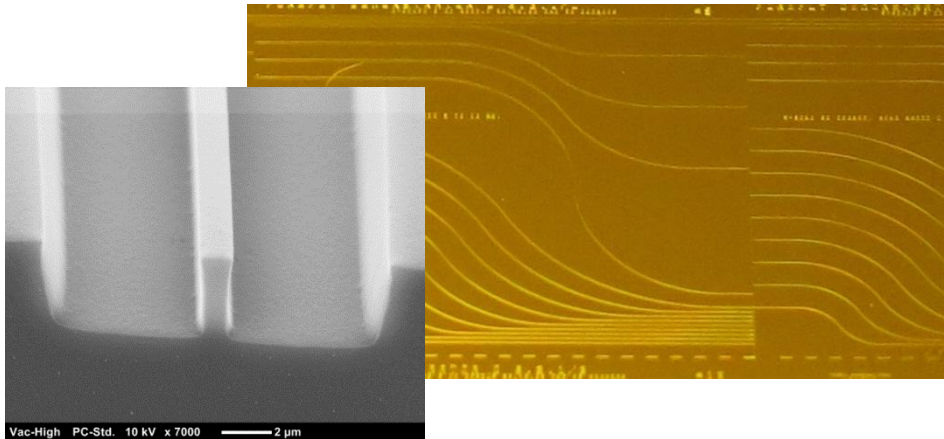
MOMENTIVE™

 **VTT**

 **VERTILAS®**

- ✿ Develop polymeric, SM waveguides and PhC structures for optical data transfer
 - based on 3D structured nano-materials
 - manufactured using new cost effective production processes
 - suitable for large scale manufacturing
- ✿ Develop new optical components (VCELS, Waveguide-fibre coupling)
- ✿ Develop new integration concepts

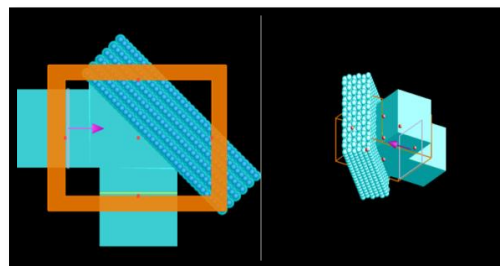
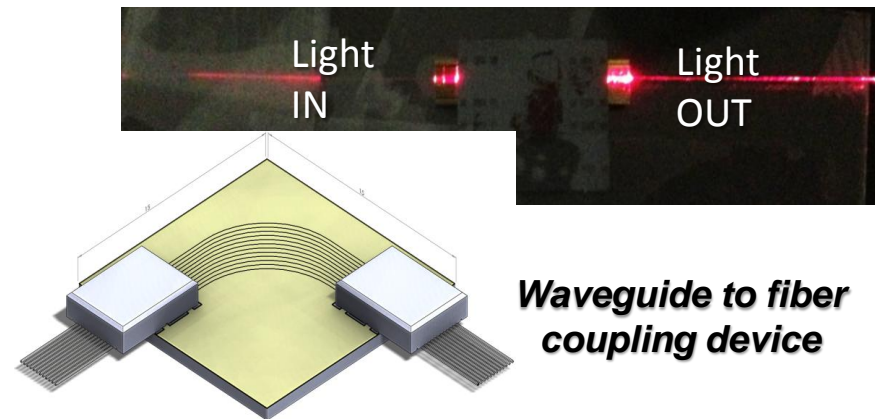
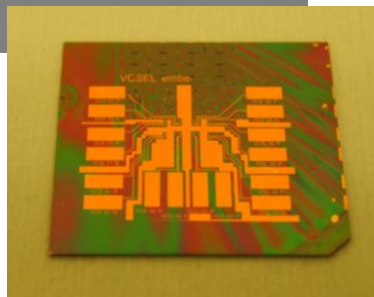




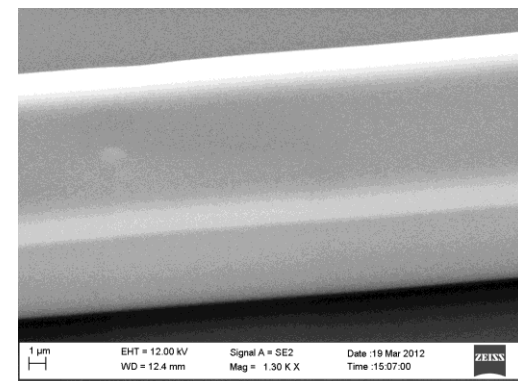
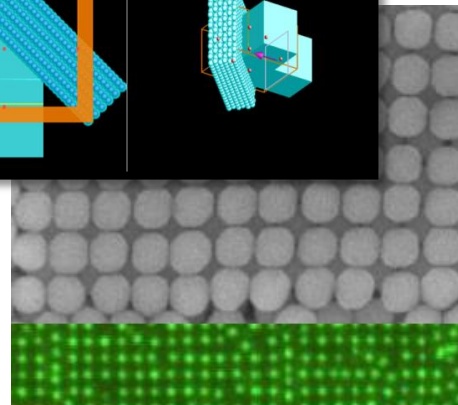
***Inverted waveguides imprinted
in siloxane polymer***



***Integration
of long wavelength
VCSELs***



Multilayer colloidal crystals

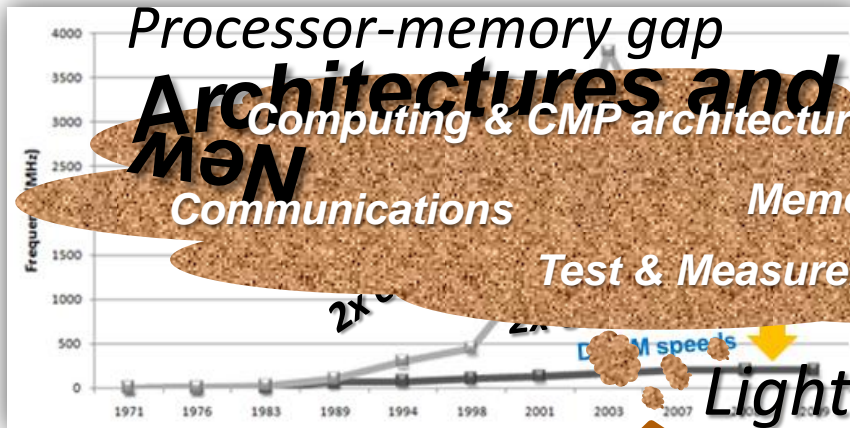


***Waveguide defined by laser
direct write photolithography***

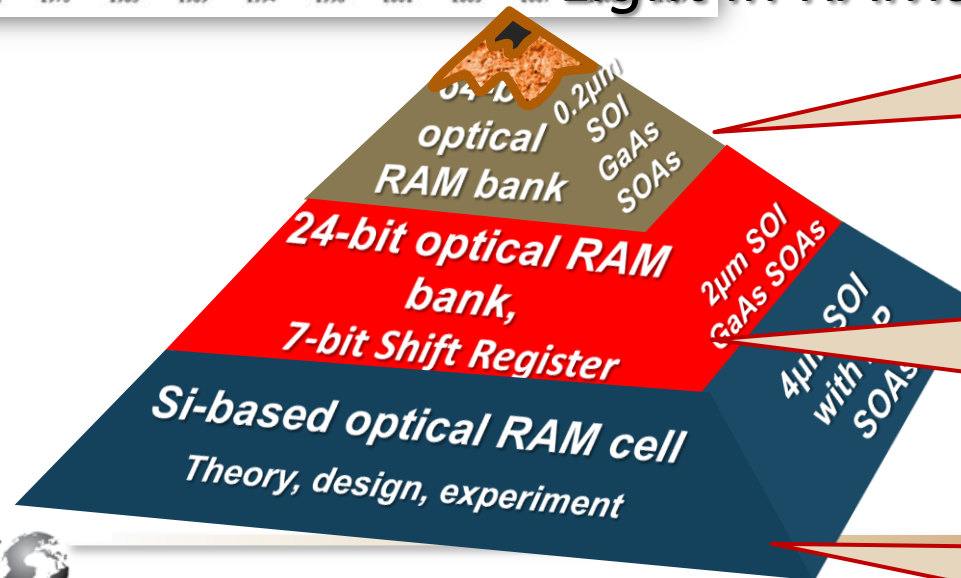
coordinated by CERTH, Greece



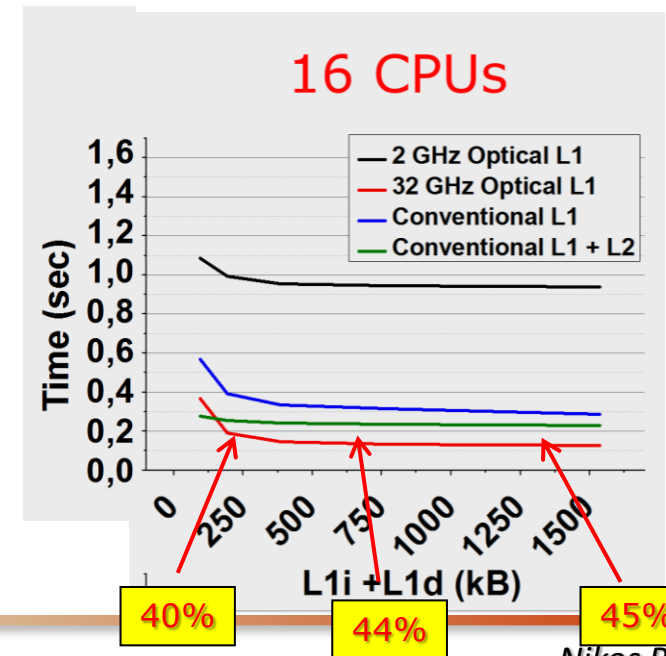
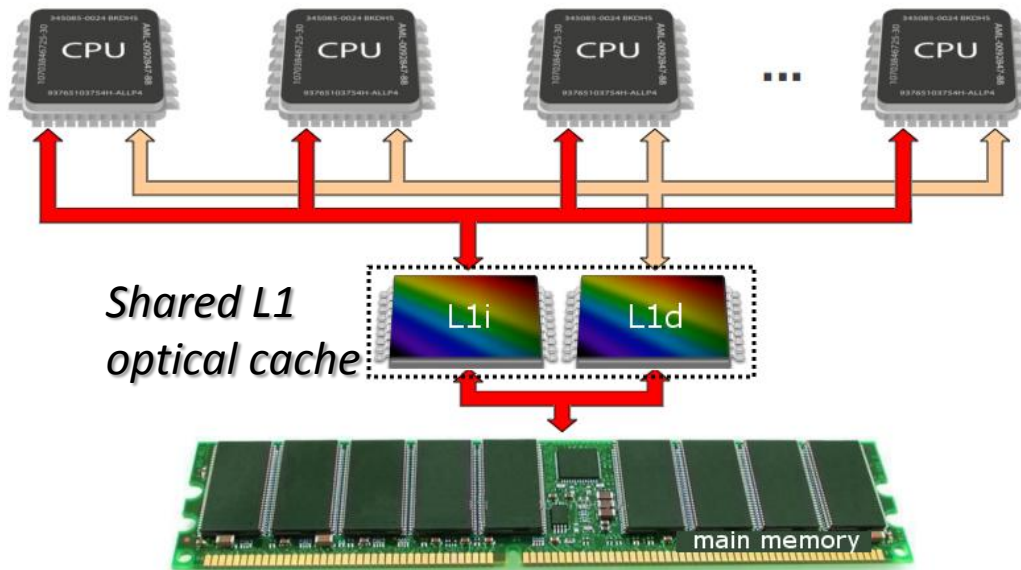
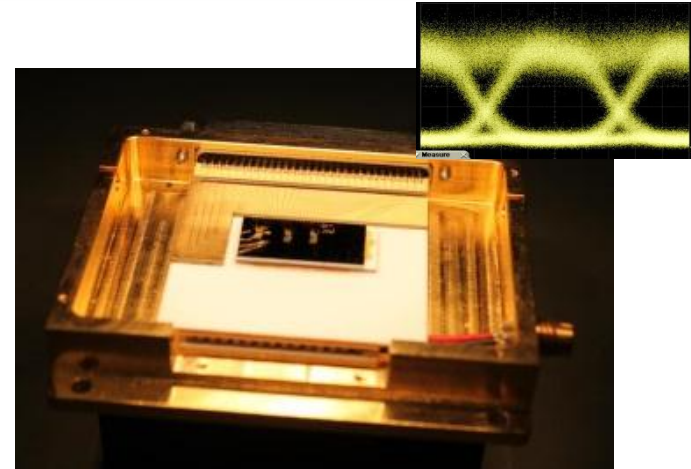
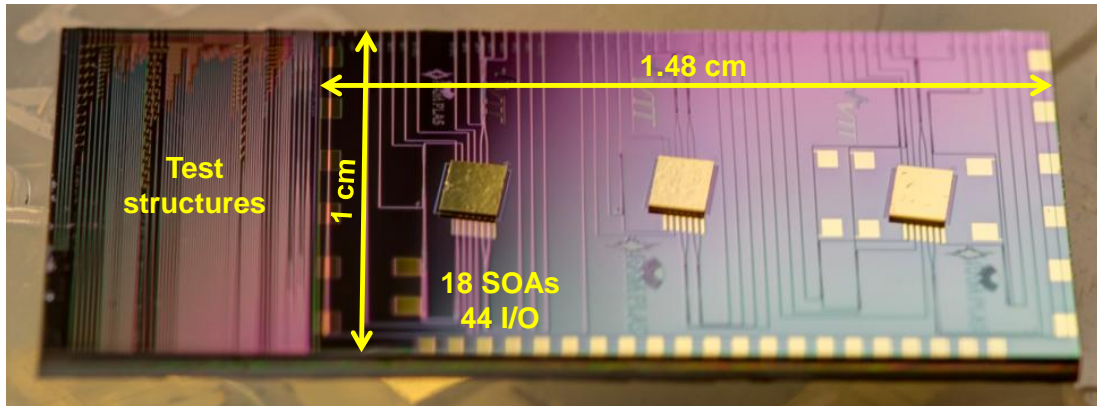
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RESEARCH & TECHNOLOGY
THE CERTH LOGO



Light in RAMs?



- ✓ Higher functionality
- ✓ Higher Integration densities
- ✓ Higher Speeds
- ✓ Lower Footprint
- ✓ Lower Power consumption
- ✓ >40GHz speeds
- ✓ On-chip optical RAM



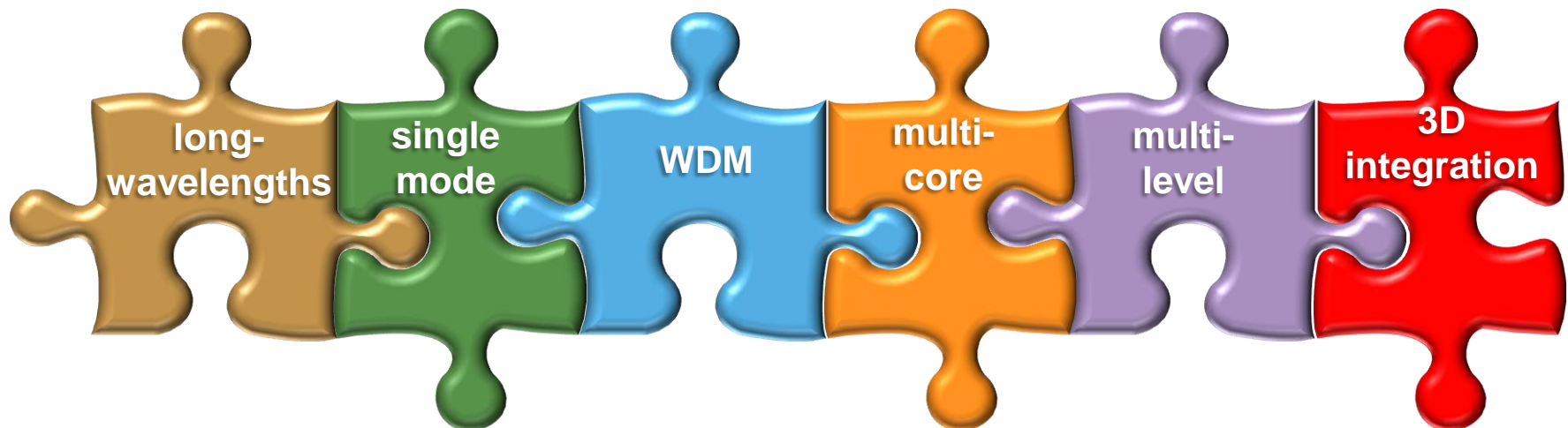


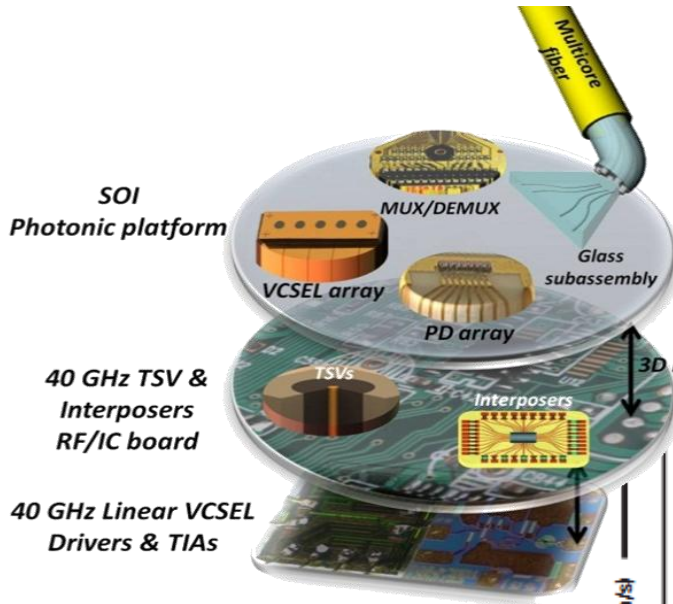
<http://www.ict-mirage.eu/>

coordinated by ICCS/NTUA, Greece

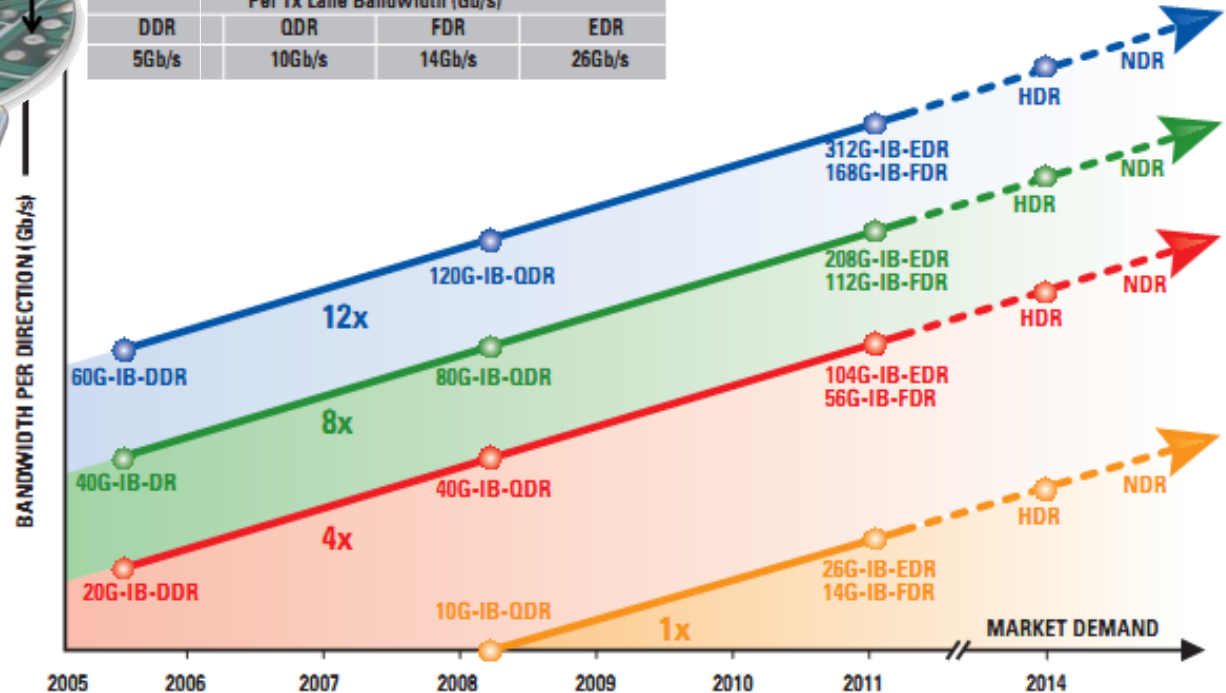


Multi-coRe,multi-level,WDM-enAbled embedded optical enGine for Terabit board- to-board and rack-to-rack parallel optics



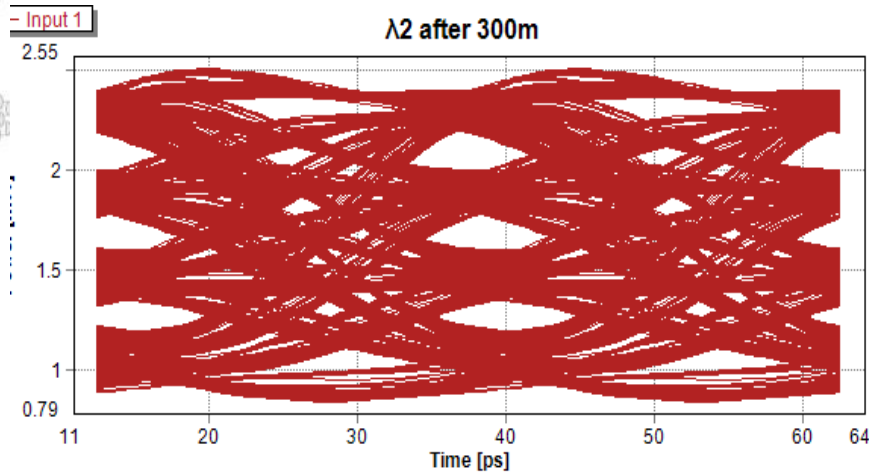
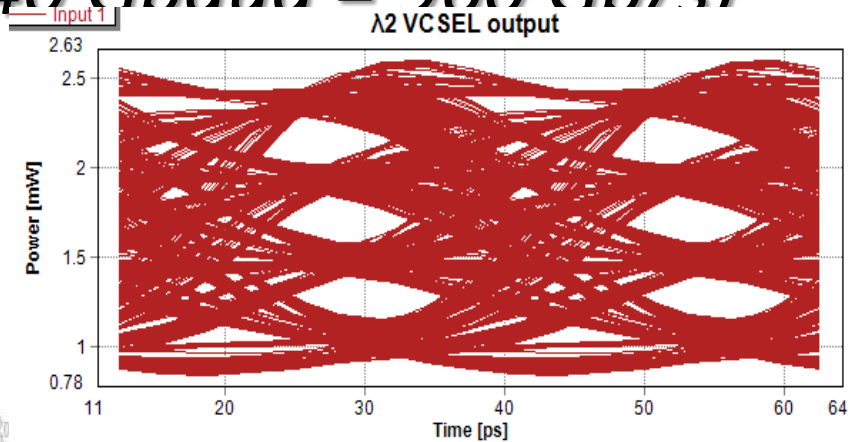
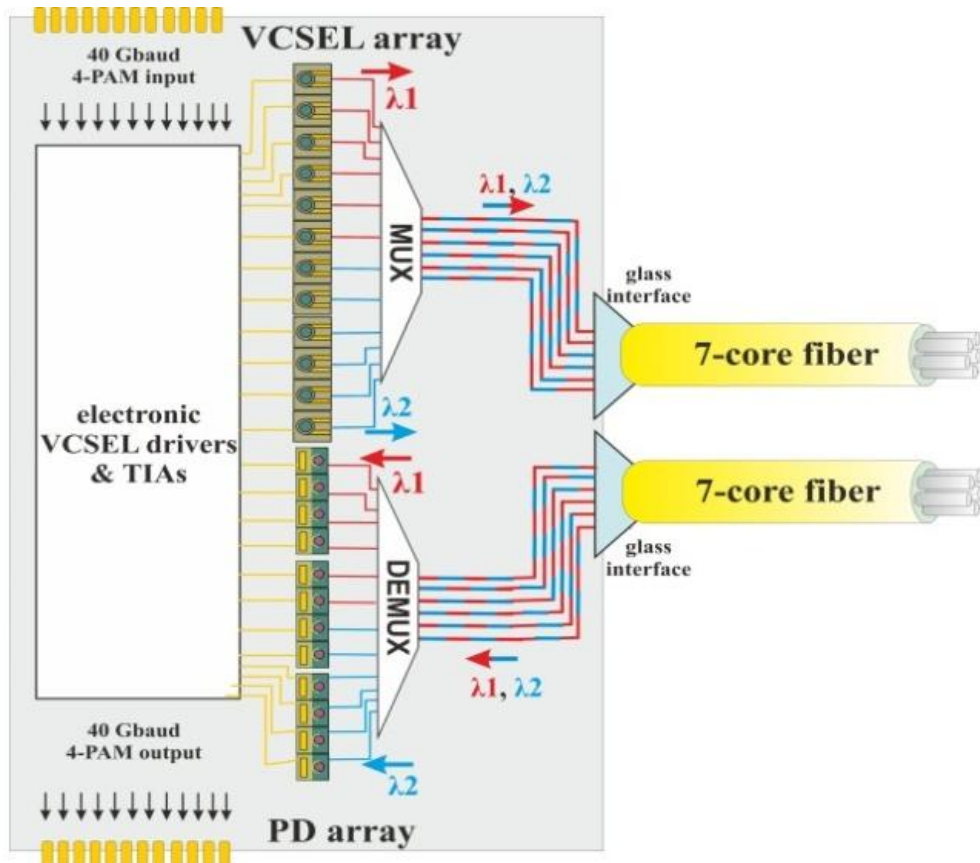


| Per 1x Lane Bandwidth (Gb/s) | | | |
|------------------------------|--------|--------|--------|
| DDR | QDR | FDR | EDR |
| 5Gb/s | 10Gb/s | 14Gb/s | 26Gb/s |



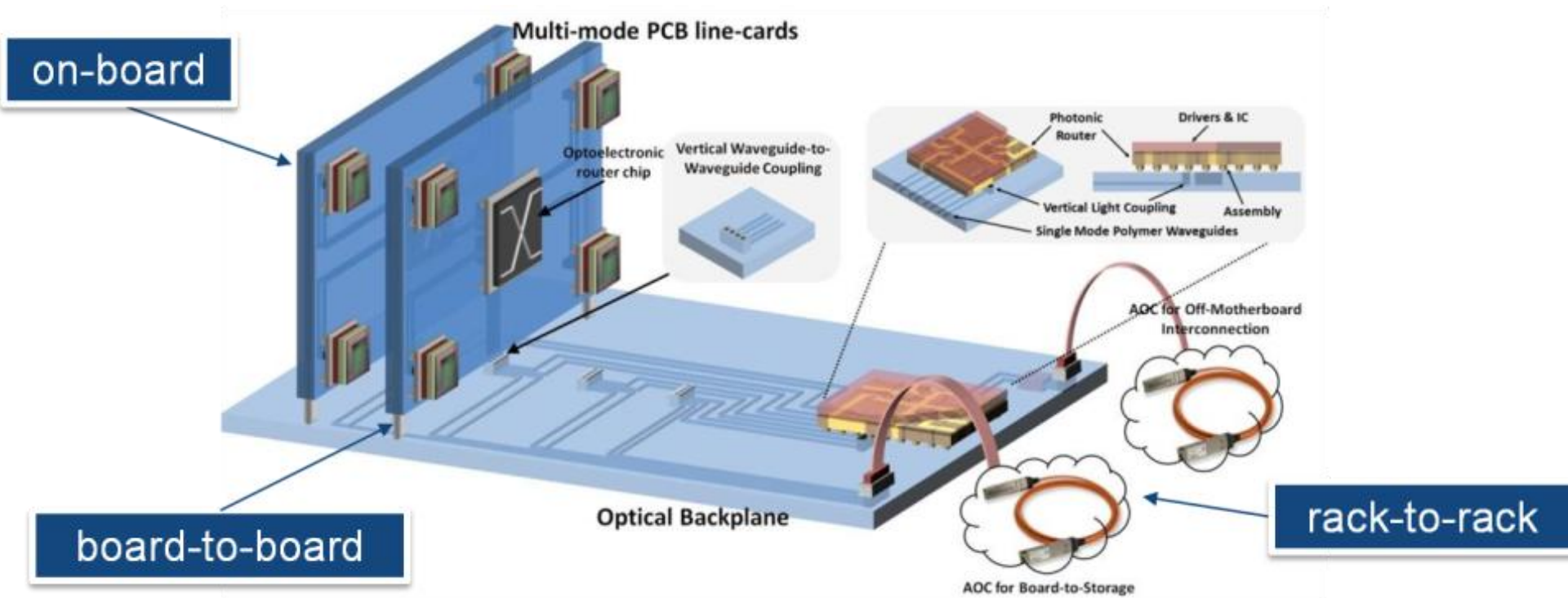


CXP AOC (6 cores x 2 λ s x 40 Gbaud = 960 Gb/s)





IP, coordinated by Fraunhofer IZM, Germany



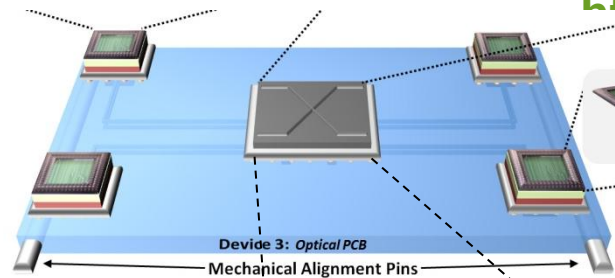


PhoxTroT

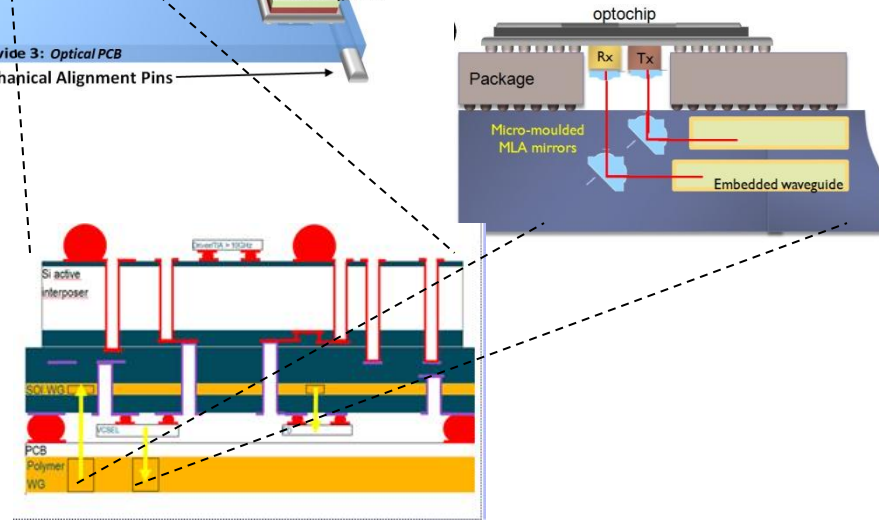
Photonics for High-Performance, Low-Cost & Low-Energy
Data Centers, High Performance Computing Systems:
Terabit/s Optical Interconnect Technologies for On-Board,
Board-to-Board, Board-to-Board, and Off-Board

<http://www.phoxtrot.eu/>

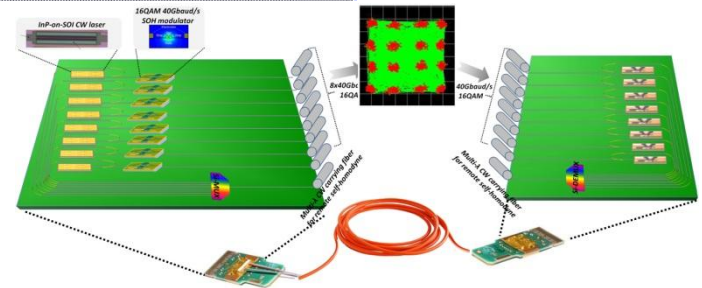
Optical PCBs



Optochips & interfaces



1.28Tb/s, 16-QAM SOI AOC



... "blending" many photonic technologies (SOI, III-V, polymer, glass, plasmonics, electronics)

Which hierarchy level ?

8 projects

3 hierarchy levels (chip-, board-, rack-level)



POLYSYS

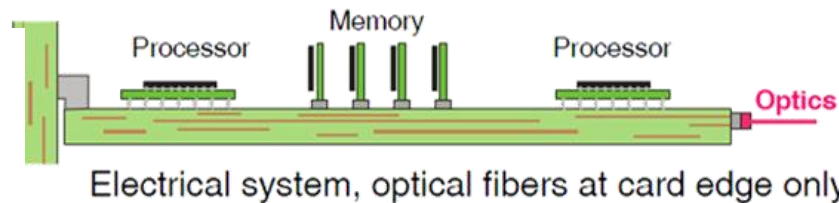


RAM PLAS



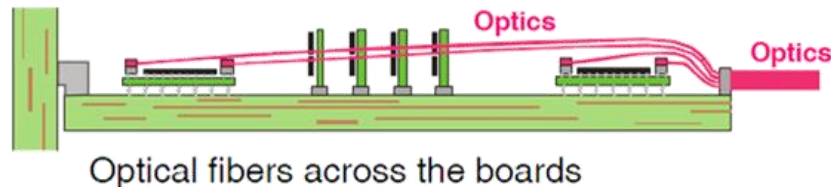
since
~2005

Backplane

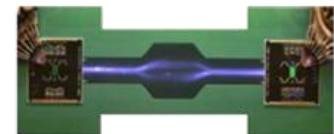
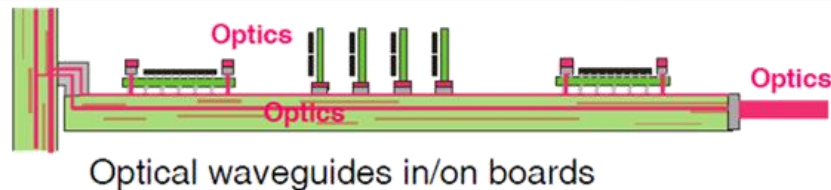


Development

Today

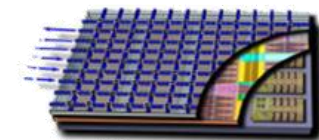
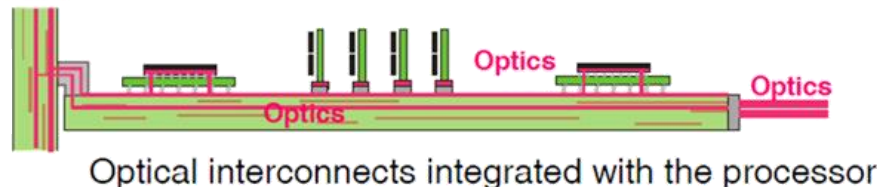


2016



Research

> 2020



Source: IBM, B. Jan Offrein, "Silicon Photonics Packaging Requirements", Munich 2011

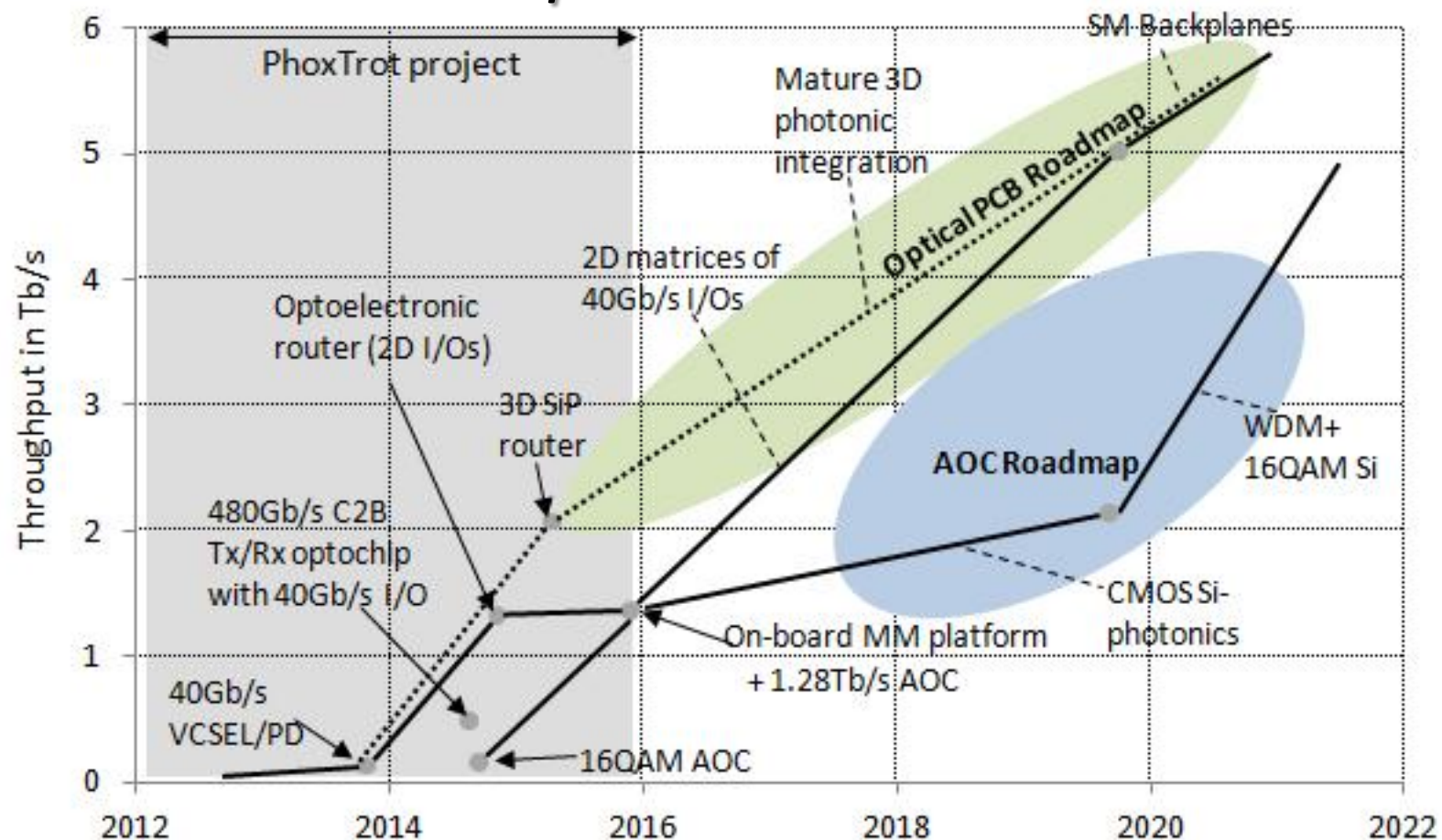
Why it matters

- ❖ ***More projects targeting R&D >2020 (on-chip)***
- ❖ ***Only a few (and new) being on today's closer-to-the-market areas (AOC and optical PCBs)***
 - ❖ *while US had already started by 2005 (IBM TeraBUS)*
- ❖ ***Much effort relies on more “disruptive” technologies (plasmonics, PhC, RAMs..)***
 - ✓ *Forward-looking, more open-ended research*
 - ✗ *Given the small total number of projects, the closer-to-the-market areas are under-supported*

cannot support a focused interconnect technology sector

How should this be done?

PhoxTrot's roadmap



Possible Actions

- *Push Photonics21 for more balanced CfPs targeting all OI hierarchical levels*
- *Strengthen synergies between architecture- (i.e. Lightness, Cosine etc) & technology-oriented projects*
- *Bring together people from different technological sectors (like III-V, SOI, polymer, glass, systems, end-users etc.)*
- *...additional ideas more than welcome !!*

THANK YOU

Upcoming events



Technology Workshop
“Optical Interconnect in Data Centers”

18-19 March 2014
Berlin, Germany

Held in conjunction with Laser Optics
www.laser-optics-berlin.de

1st European Summer School on
“Optical Interconnects”

3-6 June 2014
Thessaloniki, Greece

*Co-organized by FP7 PhoxTrot and
ECO cluster*